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iSBC® 186/51S COMMputer™ BOARD HARDWARE REFERENCE MANUAL

Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

Order Number: 122267-001

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COMMputer™ BOARD
HARDWARE REFERENCE MANUAL

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CHAPTER 1. GENERAL INFORMATION

1.1 Introduction

The iSBC 186/51S COMMputer Board is a single-board that allows Intel MULTIBUS users access on the Ethernet. The board replaces or can be used in place of the combination of an iSBC 550 board set and an iSBC 86/30 board.

The board is fully compatible with the MULTIBUS interface and can be configured for operation in a multimaster system environment. The on-board dual port RAM is expandable via the installation of an iSBC 304 plug-in memory expansion board. As shipped the RAM is totally configured as a dual-port resource. The RAM may be configured to be inaccessible from the MULTIBUS in increments of one-quarter, one-half, three-quarters or all of the total RAM size.

The iSBC 186/51S board provides a complete computer system, designed around an Intel 16-bit iAPX 186 (80186) Microprocessor and the 82586 Local Communications Controller (LCC). The 80186 microprocessor operates at a 6 MHz clock rate when performing both 8 and 16-bit data transfers.

The 82586 LCC is the Ethernet processor. The LCC gains access to the serial link, formats data and moves data to and from memory.

The iSBC 186/51S board is shipped with six sockets (arranged in three pairs) for installation of up to 192K Bytes of user provided local memory. The local memory can be configured, by jumpers to accept several devices: ROM (Read Only Memory), EPROM (Erasable Programmable Read Only Memory), RAM (Random Access Memory), and iRAM (Integrated RAM) devices. Device types can be mixed between pairs but not in a pair.

The board has the Ethernet port and two additional serial ports: an RS232C and an RS422A interface are available at connectors J1 and J2 through an 8274 Multi-Protocol Serial Controller.

Two iSBX Bus Interface connectors (J4 and J5) are provided by the board for either 8-bit or 16-bit MULTIMODULE expansion.

NOTE

Due to the use of the MB502A adapter only connector J4 is available for single-wide boards.

Figure 1-1 is a block diagram of the iSBC 186/51S board.

1.2 Description

The features of the iSBC 186/51S board are listed below and described in the text that follows:

- Full MULTIBUS interface compatibility.
- 80186 CPU providing operation at 6-MHz clock generation.
- 128K Bytes of dual port RAM available on the iSBC 186/51S board, expandable to 256K Bytes, maximum, with on-board refresh.
- 8203 Dynamic RAM Controller
- Dual Port memory addressable in either 1M Byte or 16M Byte address space from the MULTIBUS.
- Six (three pairs) JEDEC compatible 24/28 pin sockets for installation of up to 192K Bytes of local memory, plus 16K Bytes of iRMX 86 operating system kernel memory on the 80130A device.
- Two iSBX connectors (J4 and J5) to provide either 8-bit or 16-bit interfaces to MULTIMODULE boards. Only J4 can be used in the iSBC 186/51S configurations, see NOTE in Section 1.1.
- Two serial I/O channels based on the 8274 Multi-Protocol Serial Controller. One channel (J1) is RS232C/RS422A, the other channel (J2) is RS232C.

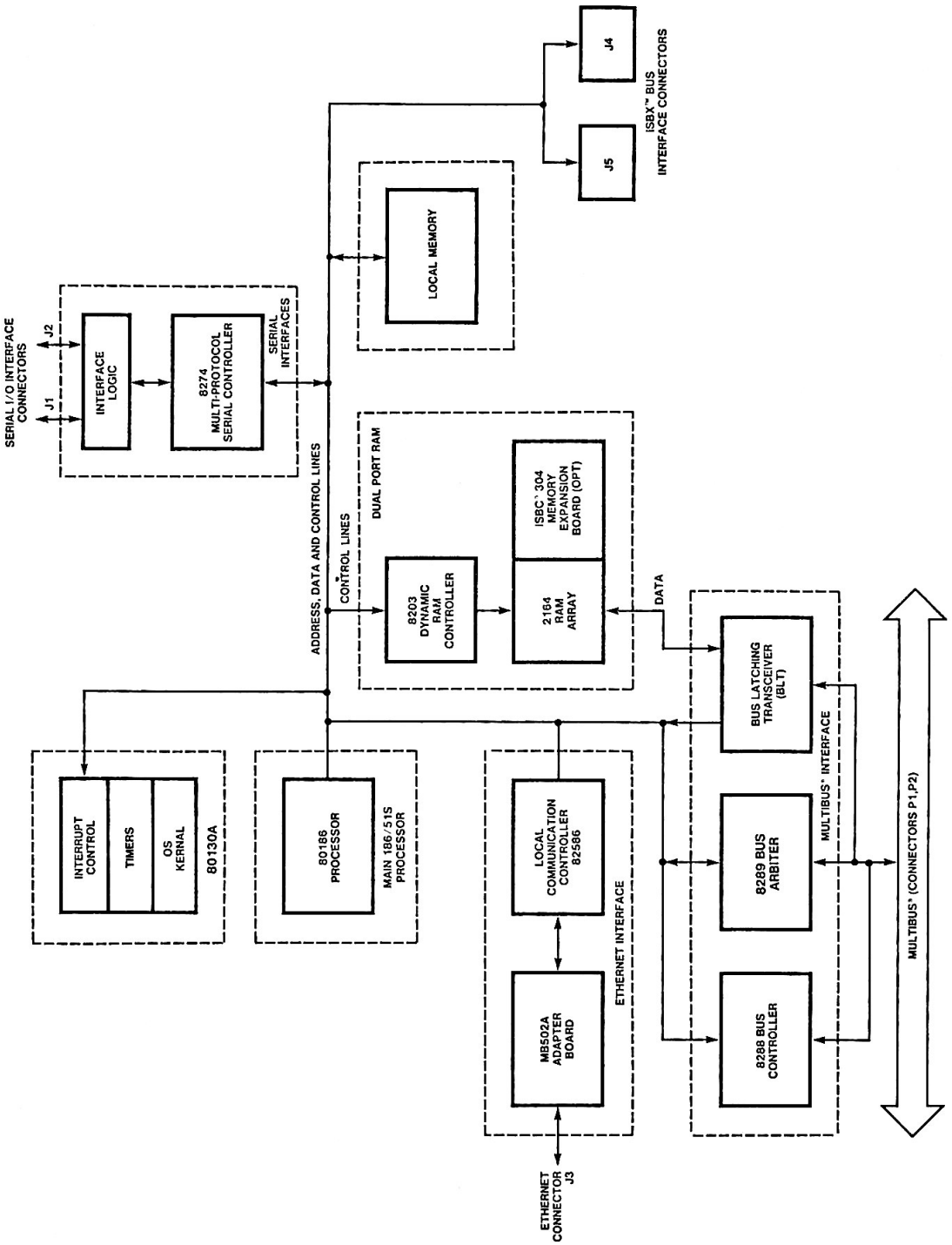


Figure 1-1. iSBC® 186/51S COMMputer™ Board Simplified Block Diagram

The 80186 Microprocessor is a 68-pin VLSI device that provides an interface with either 8 or 16 bit systems. The 80186 is configured on the iSBC 186/51S board for Maximum Mode Operation that requires the use of an 8288 Bus Controller and an 8289 Bus Arbiter device.

The 80186 CPU contains eight 16-bit general purpose registers used to contain arithmetic and logical operands. Four of these registers can be used as 16-bit registers or split into pairs of separate 8-bit registers. Four of the general purpose registers are used as base and index registers to determine offset addresses of operands in memory. Four 16-bit special registers which act as segment registers, allowing extended access to a full 1M Byte of memory addresses as well as two 16-bit special purpose registers, the status word register and the instruction pointer register. The 80186 CPU supports a wide range of addressing modes and data transfers. The 80186 CPU architecture provides several data transfer features including instruction look ahead, dynamic code relocation and re-entrant code execution.

The 82586 LCC, a 48-pin device, is an intelligent, high-performance local communications controller. It is designed to relieve the 80186 CPU of many of the tasks associated with controlling a local network and serial backplane.

The 82586 LCC upon command from the 80186 CPU moves data from memory, gains access for the Ethernet serial link, formats the data into packets and targets the data to its destination. In a receive operation, (upon command from the 80186 CPU) the LCC detects the beginning of a packet, performs address checking and moves data to memory. Further interruption from the 80186 is not required after the initial command.

The shared data bus of the 80186 and the 82586 is sixteen bits wide. The system memory can be accessed by either the 80186 or the 82586. Bus arbitration is resolved by the 80186.

The dual port control logic on the board allows the on-board RAM to communicate with the MULTIBUS interface. The board can then function as a slave RAM device when it is not controlling the MULTIBUS interface. The 80186 Microprocessor has priority when accessing the on-board RAM.

The slave RAM feature on the board can be configured to allow either 0, 32, 64, 96, or 128K Byte access by another bus master. If the iSBC 304 RAM Expansion MULTIMODULE Board is installed, the dual-port memory increments are 0, 64, 128, 192, or 256K Bytes. Thus, the board can be configured to allow other MULTIBUS Masters to access a segment of the on-board RAM and still reserve another segment for on-board use.

Six 28-pin IC sockets (JEDEC), arranged as three pairs, are included to accommodate a mix of user installed memory devices. The devices can be ROM, EPROM, RAM, or iRAM. Configuration jumpers allow the local memory to be installed in 4, 8, 16, or 32K Bytes. 2K Byte devices can be supported. However, they will appear twice in the 4K address space provided. The 80130A operating system firmware cannot be used when memory devices smaller than 8K Bytes are used. The board memory address decoding scheme assumes that the two sockets providing the low and high byte of any word access contain the same memory device. That is, there is no mixing of device types within a local memory socket pair. Jumpers permit the mixing of memory devices between local memory pairs.

Two iSBX interfaces are available on the iSBC 186/51S board via connectors J4 and J5. Only J4 can be used due to the MB502A Adapter. Each is capable of receiving either an 8- or 16-bit iSBX MULTIMODULE board. The iSBX Bus connector allows board functionality to be expanded with the installation of MULTIMODULE boards such as the iSBX 311 Analog Input MULTIMODULE board, the iSBX 328 Analog Output MULTIMODULE Board, the iSBX 350 Parallel I/O MULTIMODULE Board, the iSBX 351 Serial I/O MULTIMODULE Board, the iSBX 331 Fixed/Floating Point Math MULTIMODULE Board, the iSBX 332 Floating Point Math MULTIMODULE Board, and others.

1.3 Equipment Supplied

Each iSBC 186/51S board is shipped with a current revision of the schematic diagram. Insert the drawing into this manual for future reference. No other equipment is provided with the iSBC 186/51S board.

1.4 Equipment Required

Because the iSBC 186/51S board is designed to satisfy a variety of applications, the user must purchase and install only those components required to satisfy his particular needs. Chapter 2 provides a list of components required to configure the iSBC 186/51S board.

1.5 Optional RAM Expansion

Adding the optional iSBC 304 RAM Expansion MULTIMODULE allows the on-board RAM of the iSBC 186/51S to be expanded by 128K Bytes. Total RAM with the iSBC 304 installed is 256K Bytes. Appendix A provides instructions for installing the iSBC 304 board.

1.6 Specifications

Table 1-1 lists the specifications for the iSBC 186/51S board.

Table 1-1. Specifications

WORD SIZE		
Data	8/16 bits	
SYSTEM CLOCK SPEED	6.00 MHz	
MEMORY RESPONSE TIME	Access Time (max)	Cycle Time (min)
RAM	–	750ns nominal
Universal Memory Sites (Jumper Selectable)	200ns 350ns	500ns 625ns
LOCAL MEMORY ARRAY		
On board ROM, EPROM, iRAM	Six chip sockets, user provided memory devices in 4K x 8-bit, 8K x 8 bit, 16K x 8 bit or 32K x 8 bit capacities. ROM, EPROM, iRAM are currently supported.	
On board Dynamic Dual Port RAM	128K Bytes of dynamic RAM (256K Bytes if iSBC 304 RAM Expansion MULTIMODULE Board is installed). Data integrity maintained during power failure with user furnished batteries.	
Off Board Expansion	Up to 16M Bytes of user specified combination of RAM, ROM, and EPROM.	
MEMORY ADDRESS RANGES		
On Board Local Memory	F8000(H) - FFFFF(H) (using 4K devices). F0000(H) - FFFFF(H) (using 8K devices). E0000(H) - FFFFF(H) (using 16K devices). C0000(H) - FFFFF(H) (using 32K devices). (See Figure 3-1)	
On Board Dual Port RAM (Local 80186 CPU Access)	00000(H) - 1FFFF(H) (as shipped). 00000(H) - 3FFFF(H) (if iSBC 304 MULTIMODULE Board is installed).	
On Board RAM (MULTIBUS Interface Access)	Jumpers allow the board to act as slave RAM device for access by another bus master	

Table 1-1. Specifications (Cont'd.)

MULTIBUS Dual Port RAM Addresses	MULTIBUS addresses for the dual port RAM may begin at any 32K boundary (iSBC 304 not installed) within any 1M Byte segment of 16M Bytes of system address space. RAM is removed from the dual port in increments of 32K (e.g., either 0, 32, 64, 96, or 128K). If the iSBC 304 board is installed, MULTIBUS addresses for the dual port RAM may begin at any 64K boundary within any 1M Byte segment of 16M Bytes of system address space. RAM is removed from the dual port in increments of 64K (e.g., either 0K, 64K, 128K, 192K, and 256K. In either case, iSBC 304 installed or not, the MULTIBUS address for the dual port RAM must not overlap a 256K Byte boundary.
I/O CAPABILITY	
Parallel	Eight parallel output bits dedicated for on-board function.
Serial	One programmable RS232C interface using the 8274 Multi-Protocol Serial Controller; one programmable RS232C/RS422A using the 8274 device.
Expansion	Two iSBX Bus Connectors providing expansion via either single wide or double-wide, 8-bit or 16-bit MULTIMODULE boards. In the iSBC 186/51S application only one connector is useable.
SERIAL COMMUNICATIONS CHARACTERISTICS	
Synchronous	5- to 8-bit characters; internal or external character synchronization; automatic sync bit insertion.
Asynchronous	5- to 8-bit characters; break character generation; 1 1/2 or 2 stop bits, start-up detection.
Baud Rate	8274 Asynchronous: 19,200, 9,600, 4,800, 2,400, 1,200, 600, 300 8274 Synchronous: 125,000, 64,000, 48,000, 19,200, 9,600

Table 1-1. Specifications (Cont'd.)

MULTIBUS Interface	The iSBC 186/51S board conforms to all AC and DC requirements outlined in Intel MULTIBUS Specification, order No. 9800683-003 except for the following signals: Signal — iSBC 186/51S Board — MULTIBUS Spec. IOWC/ I_{IH} = 145µA — I_{IH} = 125µA MRDC/ I_{IH} = 165µA — I_{IH} = 125µA INIT/ I_{IH} = 70µA — I_{IH} = 50µA ADR12/-ADR17/ $-I_{IL}$ =-0.87µA — I_{IL} = -0.8µA
PHYSICAL CHARACTERISTICS	
Width	30.48 cm (12.00 inches).
Length	17.9 cm (7.05 inches).
Thickness	2.79 cm (1.1 inches) with MB502A Installed.
ENVIRONMENTAL REQUIREMENTS	
Temperature Operating	0 to 50°C at 200 LFPM.
Temperature Nonoperating	-40 to 65°C
Relative Humidity Operating	10% to 90% non-condensing.
Relative Humidity Nonoperating	5%to 95% non-condensing.
ELECTRICAL CHARACTERISTICS	
DC Power Requirements	**Maximum Current**
iSBC 186/51S Board As Shipped	+5V — +12V — -12V
Board Total (W/O Batt. Backup)	6.3A — 0.04A — 0.04A
Board Total (with Batt. Backup)	7.46A — 0.04A — 0.04A
Battery Back-up Bus	1.16A — — — —
With iSBC 304 Board Installed	+5V — +12V — -12V
Board Total (W/O Batt. Backup)	7.4A — 0.04A — 0.04A
Board Total (with Batt. Back-up)	9.26A — 0.04A — 0.04A
Battery Back-up Bus	1.86A

NOTES:
1. Add additional currents for each memory device installed in the six available Universal Memory Sites
2. Add 500 mA to +12V current if Ethernet transceiver is connected.
3. Add additional currents for any iSBX modules installed.

1.7 List of Abbreviations

The following list contains the signal mnemonics and abbreviations used throughout this manual and on the engineering drawing. Active state indicators (slash (/) for low level, no slash for high level) are not provided for signal names or mnemonics.

ACK	Acknowledge
ADEN	Address Enable
ALE	Address Latch Enable
BHEN	Byte High Enable
BPRN	Bus Priority In
BPRO	Bus Priority Out
BREQ	Bus Request
BUSDEN	Bus Data Enable
CLK	Clock
CMD	Command
CS	Chip Select
CTS	Clear To Send
DEN	Data Enable
DMA	Direct Memory Access
DP	Dual Port
DSR	Data Set Ready
DT/R	Data Transfer/Receive
DTR	Data Terminal Ready
EN	Enable
ESI	Ethernet Serial Interface
INT	Interrupt
IOWC	Input/Output Write Command
IORD	Input/Output Read Command
MEM	Memory
MWTC	Memory Write Command
MRDC	Memory Read Command
NMI	Non-Maskable Interrupt
NVEN	Non-Volatile Memory Enable
OB	On-Board
ONBDDT/R	On-Board Data Transfer/Receive
PAL	Programmable Array Logic
PROC LOCK	Processor Lock
PROM	Programmable Read Only Memory
PU	Power Up

RAM	Random Access Memory
RDY	Ready
REQ	Request
RXC	Receive Clock
RXD	Receive Data
SACK	System Acknowledge
SBC	Single Board Computer
TMR	Timer
TXC	Transmit Clock
TXD	Transmit Data
WT	Write
XACK	Transfer Acknowledge

CHAPTER 2. PREPARATION FOR USE

2.1 Introduction

This chapter provides instructions for preparing the iSBC 186/51S board for use in a user defined environment. This chapter includes unpacking and inspection instructions, installation considerations, component installation, jumper configuration, interface configuration for the MULTIBUS, the iSBX bus and the serial bus interfaces and connector information.

2.2 Unpacking and Inspection

Upon receiving the iSBC 186/51S board from the carrier, immediately inspect the shipping container for damage. If the shipping container is damaged or water stained, request the carrier's agent to be present when the carton is opened; if the carrier's agent is not present at the time of opening, keep the container and packing material so the agent can inspect it at a later date.

When the container is opened, verify the contents with the shipping list. Remove all packing material from the board(s). Check each board for physical damage such as broken components. Certain damage such as a cracked printed circuit board or failing integrated circuit may not be detected until power is applied and tests are conducted on the unit. If you discover physical damage or the board fails after installation, refer to Chapter 5, "Service and Repair Assistance."

2.3 Installation Considerations

Installation considerations such as power, cooling and physical size requirements are outlined in the following paragraphs.

NOTE

The iSBC 186/51S board includes a large number of stake pins that can be connected (jumpered) for various board configurations. Tables 2-4, 2-5, and 2-22 through 2-32 list and define the various jumper functions. Table 2-22 lists all stake pins and locates them in their respective tables and on the schematic diagram (see Section 5). Table 2-22 also indicates the default jumpers (those installed by the factory).

2.4 DC Power Requirements

Power requirements for the iSBC 186/51S board are shown in Table 2-1. Power requirements for both the system bus and the battery backup bus are provided. Current requirements shown in the table do not include the current required by byte-wide devices. To determine the total power requirements for unique applications add the current required by user installed devices and boards to the values shown in Table 2-1.

Table 2–1. DC Power Requirements

Parameter	Maximum Current		
	+5V	+12V	-12V
iSBC 186/51S Board as Shipped			
Board Total w/o Battery Backup	6.3A	0.04A	0.04A
Board Total with Battery Backup	7.46A	0.04A	0.04A
Battery Backup Bus	1.16A	-	-
iSBC 304 Memory Module Installed			
Board Total w/o Battery Backup	7.4A	0.04A	0.04A
Board Total with Battery Backup	9.26A	0.04A	0.04A
Battery Backup Bus	1.86A	-	-

NOTES:
1. Add additional currents for each memory device installed in the six available Universal Memory Sites.
2. Add 500 mA to +12V current if Ethernet transceiver is connected.
3. Add additional current for any iSBX modules installed.

2.5 Cooling Requirements

Adequate air circulation must be provided to prevent the temperature from rising above 50°C. Board heat dissipation is shown below.

Configuration	Watts	gm cal/min	BTU/min
As shipped	26.5	376	1.51
With Devices Installed in Universal Memory Site	31.0	440	1.76
With Devices Installed in Universal Memory Site and iSBC 304 board installed	31.5	447	1.79

2.6 Physical Dimensions

The outside dimensions of the iSBC 186/51S board are:

Width 30.48 cm (12.00 inches).
Length 17.9 cm (7.05 inches).
Thickness 2.79 cm (1.1 inches).

2.7 User Furnished Components

Table 2-2 lists the user furnished components required to configure all intended applications of the iSBC 186/51S board. Table 2-3 lists the connector manufacturers from who you may obtain parts to interface with P1, P2, J1, J2, J3, J4 and J5 connnectors on the iSBC 186/51S board. Paragraphs 2-14 and 2-15 lists the cable configuration information for serial connector J1 and J2 and Ethernet connctor J3 respectively. Figure 2-1 shows the mounting location on the iSBC 186/51S board for each of the user provided components. You need only install those components required to satisfy an application. Figure 2-1 also shows all major components and all stake pin locations for the board.

Table 2-2. User Furnished Components

Item No.	Item	Description	Function
1.	Connector (Mates with P1)	See MULTIBUS Connector details in Table 2-3.	Power inputs and MULTIBUS signal Interfaces.
2	Connector (Mates with P2)	See MULTIBUS Connector details in Table 2-3.	Auxiliary battery backup and associated protection functions.
3	Connectors (Mates with J1 and J2)	See Serial I/O Connector Cable details in Table 2-3.	RS232C or RS449 connection to the iSBC 186/51S
4	Transceiver Cable ISBC 186/51S J3 and Ethernet Transducer	See Section 2-10 and Figure 2-2.	Ethernet connection to the iSBC 186/51S.
5	EPROM Chips	Up to six each of the following types: 2732 (4K x 8) 2764 (8K x 8) 27128 (16K x 8) 27286 (32K x 8)	Local Memory
6	iRAMs	Up to four each of the following types (8K x 8) (16K x 8)	Local Memory
7	Static RAMs	Up to four each.	Local Memory
8	iSBC 304 RAM MULTI-MODULE Board	128K Bytes of RAM expansion capability	Provides the capability to expand the on-board RAM to 256K Bytes.
9	Headers	Mode with Augat, Inc. Component Carrier, P/N 322-HC-5P3-10. User must install conductors as shown in Figure 2-3 and Section 2-21.	Converts serial interface from RS422A to RS232C.
10	iSBX MULTIMODULE Boards (Installed at J4, J5 not available in iSBC 186/51S configuration).	See last pargraph of Section 1.2	Expand board functionality.

Table 2-3. User Furnished Connector Information

Function	No. of Pins	Centers	Connector Type	Vendor	Vendor Number
MULTIBUS Connector	43/86	0.156 in 0.396 cm	Soldered PC Board Mount	Viking ELFAB	2KH43/9AMK12 BS1562D43PBB
			Wirewrap without Ears	EDAC ELFAB	337086540201 BW1562D43PBB
			Wirewrap with .128 DIA Mounting holes	EDAC ELFAB	337086540202 BW1562A43PBB
Auxiliary Connector	30/60	0.100 in	Soldered	ELFAB EDAC	97169001 34060524300
			Wirewrap No Ears	ELFAB EDAC	BW1020D30PBB 34506540201
			Wirewrap	ELFAB EDAC	BS1020A30PBB 345060524802
			Wirewrap with .128 DIA	TI Viking	H421121-30 3KH30/9JNK
Serial I/O Connectors J1 and J2	26	0.100 in	Right Angle	3M AMP	3399-6000
iSBX Bus Connector 8/16-bit (J4, J5)	36/44	0.100 in	Soldered	Viking	00293-0001

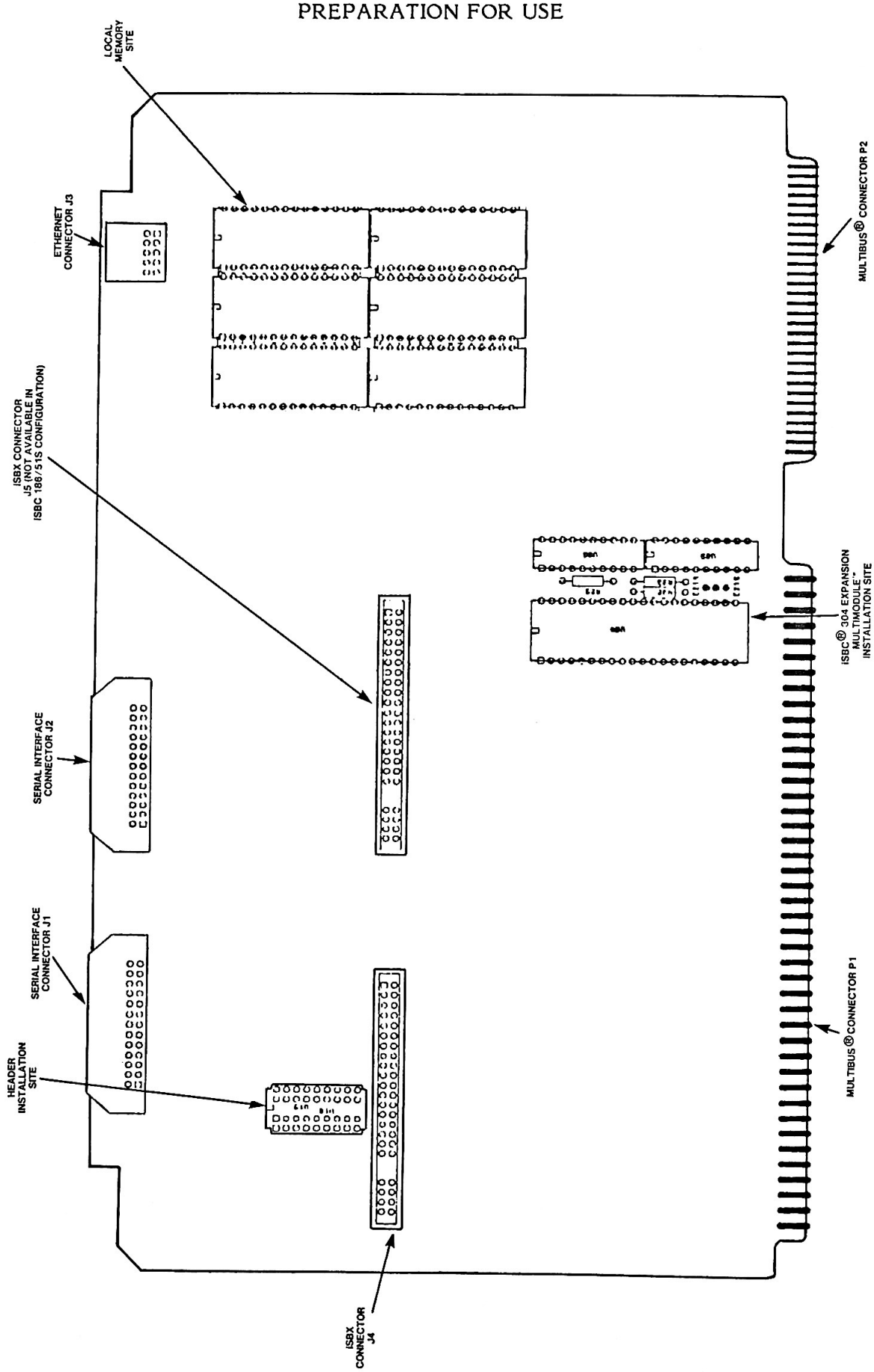


Figure 2-1. iSBC® 186/51S Board Component Locations

2.8 User Furnished Component Installation

The following paragraphs contain the instructions for installing the user provided components (EPROMS, ROMS, and iRAMS) on the iSBC 186/51S board.

CAUTION

All MOS devices such as EPROMS are highly susceptible to damage from static electricity. Use extreme caution when installing MOS devices. Always ground yourself before handling MOS devices to ensure that a static charge build-up is not dissipated through or around the MOS devices.

2.9 Local Memory Device Installation

As shipped from the factory the iSBC 186/51S board contains no local memory devices. The user may install one of several different types of memory devices into the local memory 28-pin JEDEC sites. However, the memory address configuration depends on the type of memory device selected. The local memory site consists of six sockets arranged in three pairs. Memory device type can vary between pairs but not in a pair.

The pairing of the JEDEC sockets is as follows: U32 and U49, U33 and U50, and U34 and U51. The memory size per socket can be 4, 8, 16 or 32K Bytes. The sockets are located at the top of the 1M Byte address space of the 80186 processor.

Configure the sockets (for memory device size) using the jumpers listed in Table 2-4. Jumper selection is determined by the largest memory device size in any socket. Install the remaining socket jumpers as listed in Table 2-5. The access time of the memory devices installed in a pair should then be checked against the times in Table 2-21 to determine the appropriate number of wait states.

In the standard "as shipped" configuration only socket pairs U32/U49 and U33/U50 will accept iRAMs. The timing for these socket pairs is different than the other pair. Socket pair U34/U51 cannot accept iRAMs.

Table 2-6 gives the local memory address assignments

Table 2-4. JEDEC Size Selection Jumpers

Jumper		Functions	Total Memory	Reference Schematic Figure 5-3 Sheet
E199 - E203	E191 - E199			
In*	In*	Selects 4K Memory Device Size	24K Bytes	8
In	Out	Selects 8K Memory Device Size	48K Bytes	8
Out	In	Selects 16K Memory Device Size	96K Bytes	8
Out	Out	Selects 32K Memory Device Size	192K Bytes	8

NOTE: * Indicates wirewrap jumper required.

Table 2-5. Local Memory Device Selection Jumpers

Integrated RAMs			
	U34/U51	U33/U50	U32/U49
8K and 16K Devices	-	E94 - E98	E136 - E138
	-	E107 - E108	E142 - E143
	-	E112 - E116*	E145 - E147*
EPROM			
	U34/U51	U33/U50	U32/U49
4K Devices	E110 - E114*	E112 - E116*	E145 - E147*
	E113 - E117	E115 - E119	E146 - E148
8K Devices	E91 - E92*	E93 - E94*	E135 - E136*
	E105 - E109*	E107 - E111*	E142 - E144*
	E110 - E114*	E112 - E116*	E145 - E147*
16K Devices	E91 - E92*	E93 - E94*	E135 - E136*
	E105 - E109*	E107 - E111*	E142 - E144*
	E110 - E114*	E112 - E116*	E145 - E147*
	E117 - E118	E119 - E120	E148 - E149
32K Devices	E91 - E92*	E93 - E94*	E135 - E136*
	E103 - E105	E104 - E107	E141 - E142
	E110 - E114*	E112 - E116*	E145 - E147*
	E117 - E118	E119 - E120	E148 - E149

NOTE: *Indicates default connection.

Table 2-6. Local Memory Socket Address Assignments

Sockets	Device Capacities			
	4K	8K	16K	32K
U34 / U51	FE000 - FFFFF	FC000 - FFFFF	F8000 - FFFFF	F0000 - FFFFF
U33 / U50	FA000 - FBFFF	F4000 - F7FFF	E8000 - EFFFF	D0000 - DFFFF
U32 / U49	F8000 - F9FFF	F0000 - F3FFF	E0000 - E7FFF	C0000 - CFFFF

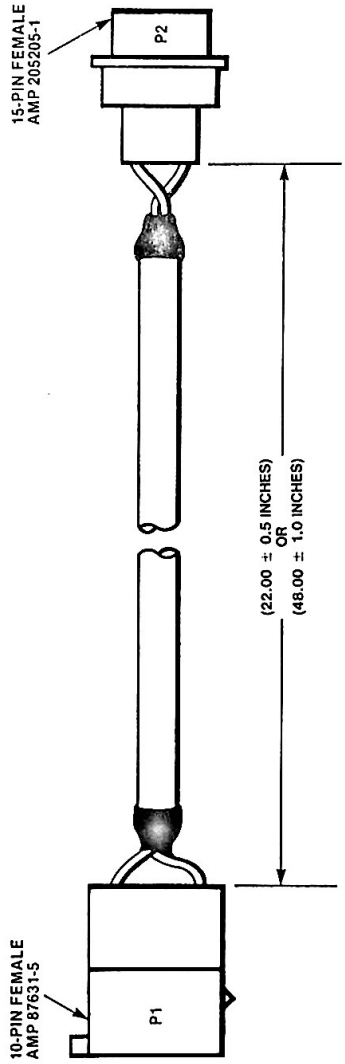
2.10 Transceiver Cable

The mating connector for the iSBC 186/51S board transceiver interface is an AMP 87631-5. The user must fabricate a suitable internal cable assembly which terminates in an Ethernet-standard 15-pin D-subminiature female connector to which commercially available transceiver cables can be attached. The internal cable should be mounted to the chassis connector panel using the sliding lock post (Cinch D53018) called out in the Ethernet specification. Figure 2-2 shows the Ethernet Internal Transceiver Cable.

2.11 Ethernet Address Selection

Ethernet processor IDs are controlled by an Ethernet Address Administrator, located at XEROX Office Product Division, System Development Department, Palo Alto California. Ethernet processor IDs consist of a string of six octets; the IDs assigned in blocks identified by a Block ID. The least significant bit of the first octet is the multicast bit; the block ID consists of the remaining 23 bits of the first three octets. The last three octets are specified by the owners of the Block IDs.

The Ethernet Address Administrator assigns the IDs using hexadecimal notation. For example, Xerox Corporation is assigned the block ID 00 00 AA and is therefore allocated the blocks represented by the hexadeximals 00 00 AA UU UU UU (for physical addresses) and 01 00 AA UU UU UU (for multicast addresses), where U represents an unspecified hexadecimal digit.



P1 Pin Number	Function		P2 Pin Number
1	Transmit +	Twisted Pair	3
2	Transmit –		10
3	Receive +	Twisted Pair	5
4	Receive –		12
5	Collision +	Twisted Pair	2
6	Collision –		9
7	+12 Vdc Return	Twisted Pair	6
9	+12 Vdc		13

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Figure 2-2. Ethernet Internal Transceiver Cable

As defined in the Ethernet Specification Version 1.0, September 30, 1982, the interpretation of the bits as transmitted on the cable is that the left-most bit (first transmitted) is the low order (2^0) digit and the right most bit (last transmitted) is the high order (2^7) digit.

Values for UU UU UU identify individual processors and are allocated to specific Ethernet Hosts or families of Hosts, as required. For Xerox products, the Ethernet Address Administrator assigns numbers to families of Xerox Hosts. Project leaders, or managers, assign numbers to individual Hosts within the family.

Requests for processor IDs for Host families should be sent to the Ethernet Address Administrator in Palo Alto. Requests must include the name of the project, the requestor's name, and organization, the name of the individual responsible for handing out the assignment, and the number of IDs required. Allocations are made in blocks represented as hexadecimal digits.

2.12 Interface Requirements

The iSBC 186/51S board interfaces are described in Section 2.13 through 2.17

2.13 MULTIBUS® Interface

Connectors P1 and P2 interface the iSBC 186/51S board to the MULTIBUS interface. Table 2-7 lists connector P1 pin assignments and Table 2-8 provides descriptions of the signal functions.

Signal names indicate the active state of the signal on the MULTIBUS interface. If the signal name ends with a slash (/), the signal is active low; if the signal does not end with a slash, the signal is active high.

The iSBC 186/51S board conforms to all AC requirements and most DC requirements outlined in the Intel MULTIBUS Specification, Order No. 9800683-03. The DC specification exceptions are listed in Table 2-9. The exceptions do not compromise MULTIBUS compatibility.

Table 2-10 lists the pin assignments for the P2 connector. Table 2-11 provides signal description for connector P2.

Table 2-7. iSBC® 186/51S Connector P1 Pin Assignments

	Pin	(Component Size)		Pin	(Solder Side)	
		Mnemonic	Description		Mnemonic	Description
Power Supplies	1	GND	Signal GND	2	GND	Signal GND
	3	+5V	+5Vdc	4	+5V	+5Vdc
	5	+5V	+5Vdc	6	+5V	+5Vdc
	7	+12V	+12Vdc	8	+12V	+12Vdc
	9		Reserved, bussed	10		Reserved, bussed
	11	GND	Signal GND	12	GND	Signal GND
Bus Controls	13	BCLK/	Bus Clock	14	INIT/	Initialize
	15	BPRN/	Bus Pri. In	16	BPRO/	Bus Pri. Out
	17	BUSY/	Bus Busy	18	BREQ/	Bus Request
	19	MRDC/	Mem Read Cmd	20	MWTC/	Mem Write Cmd
	21	IORC/	I/O Read Cmd	22	IOWC/	I/O Write Cmd
	23	XACK/	XFER Acknowledge	24	INH1/	Inhibit 1 disable RAM
Bus Controls and Address	25	LOCK/	Lock	26	INH2/	Inhibit 2 disable PROM or ROM (not used)
	27	BHEN/	Byte High Enable	28	AD10/	
	29	CBRQ/	Common Bus Request	30	AD11/	Address
	31	CCLK/	Constant Clk	32	AD12/	Bus
	33	INTA/	Intr Acknowledge (not used)	34	AD13	

Table 2-7. iSBC® 186/51S Connector P1 Pin Assignments (Cont'd.)

	Pin	(Component Size)		Pin	(Solder Side)	
		Mnemonic	Description		Mnemonic	Description
Interrupts	35	INT6/	Parallel	36	INT7/	Parallel
	37	INT4/	Interrupt	38	INT5/	Interrupt
	39	INT2/	Requests	40	INT3/	Requests
	41	INT0/		42	INT1/	
Address	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/	Address	48	ADRB/	Address
	49	ADR8/	Bus	50	ADR9/	Bus
	51	ADR6/		52	ADR7/	
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	
Data	59	DATE/		60	DATF/	
	61	DATC/		62	DATD/	
	63	DATA/	Data	64	DATB/	Data
	65	DAT8/	Bus	66	DAT9/	Bus
	67	DAT6/		68	DAT7/	
	69	DAT4/		70	DAT5/	
	71	DAT2/		72	DAT3/	
	73	DAT0/		74	DAT1/	
Power Supplies	75	GND	Signal GND	76	GND	Signal GND
	77		Reserved, bussed	78		Reserved, bussed
	79	-12V	-12Vdc	80	-12V	-12Vdc
	81	+5V	+5Vdc	82	+5V	+5Vdc
	83	+5V	+5Vdc	84	+5V	+5Vdc
	85	GND	Signal GND	86	GND	Signal GND

Table 2-8. Connector P1 Signal Descriptions

Signal	Functional Description
ADR0/-ADRF/ ADR10/-ADR13/	Address. These 20 lines transmit the address of the memory location or I/O port to be accessed. ADR13/ is the most significant address bit for 20-bit addressing.
BCLK/	Bus Clock. Used to synchronize the bus contention logic on all bus masters. When generated by the iSBC 186/51S board, BCLK/ has a period of 100.0 nanoseconds (10.00 MHz), with a 50 percent duty cycle.

Table 2-8. Connector P1 Signal Descriptions (Cont'd.)

Signal	Functional Description
BHEN/	Byte High Enable. Used to select the upper byte (bits 8 through F) of a 16-bit word. The signal is functional only in systems that incorporate 16-bit memory and I/O devices.
BPRN/	Bus Priority In. Indicates to a particular bus master that no higher priority master is requesting use of the bus. BPRN/ is synchronized with BCLK.
BPRO/	Bus Priority Out. In serial (daisy chain) priority resolution schemes, BPRO/ must be connected to the BPRN/ input of the bus master with the next lower bus priority.
BREQ/	Bus Request. In parallel priority resolution schemes, BREQ/ indicates that a particular bus master requires control of the bus for one or more data transfers. BREQ/ is synchronized with BCLK/.
BUSY/	Bus Busy. Indicates the bus is in use and prevents all other bus masters from gaining control of the bus. BUSY/ is synchronized with BCLK/.
CBRQ/	Common Bus Request. Indicates that a bus master wishes control of the bus but does not presently have control. As soon as control of the bus is obtained, the requesting bus controller releases the CBRQ / signal.
CCLK/	Constant Clock. Provides a clock signal of constant frequency for use by other system modules. When generated by the iSBC 186/51S board, CCLK/ has a period of 100.0 nanoseconds (10.00 MHz), with a 50 percent duty cycle.
DAT0/-DATF/	Data. These 16 bi-directional data lines transmit and receive data to and from the addressed memory location or I/O port. DATF/ is the most significant bit.
INH1/	Inhibit RAM. For system application, allows iSBC 186/51S board dual port RAM addresses to be overlaid by PROM in the system.
INIT/	Initialize. Resets the entire system to a known internal state.
INTA/	Interrupt Acknowledge. Not supported by the iSBC 186/51S board.
INT0/ - INT7/	Interrupt 0 through Interrupt 7. An interrupt can be generated by activating one of the eight interrupt request lines with an open collector driver. The interrupt request line are priortized with INTO/having the highest priority.
IORC/	I/O Read. Indicates that the address of an I/O port is on the MULTIBUS interface address lines and that the output of that port is to be read (placed) onto the MULTIBUS interface data lines.

Table 2-8. Connector P1 Signal Descriptions (Cont'd.)

Signal	Functional Description
IOWC/	I/O Write. Indicates that the address of an I/O port is on the MULTIBUS interface address lines and that the contents on the MULTIBUS interface data lines are to be accepted by the addressed port.
LOCK/	Lock. When another MULTIBUS master accesses the 186/51S on-board dual port RAM and activates the LOCK/ signal, the on-board resources are locked out of the dual port RAM until the LOCK/ signal is removed by the MULTIBUS master. LOCK/ can be enabled onto the MULTIBUS interface by the 186/51S to perform the same function on another dual ported RAM board.
MRDC/	Memory Read Command. Indicates that the address of a memory location is on the MULTIBUS interface address lines and that the contents of that location are to be read (placed) on the MULTIBUS interface data lines.
MWTC/	Memory Write Command. Indicates that the address of a memory location is on the MULTIBUS interface address lines and that the contents on the MULTIBUS interface data lines are to be written into that location.
XACK/	Transfer Acknowledge. Indicates that the commanded read or write operation is complete and the data has been placed on or accepted from the MULTIBUS interface.

Table 2-9. iSBC® 186/51S Board, MULTIBUS® Specification Deviation

Signal	Parameter iSBC 186/51S Board Specification	MULTIBUS Specification
IOWC/	I_{IH} = 145µA	I_{IH} = 125µA
MRDC	I_{IH} = 165µA	I_{IH} = 125µA
INIT/	I_{IH} = 70µA	I_{IH} = 50µA
ADR12/-ADR17/	I_{IL} = 0.87mA	I_{IL} = 0.80mA

Table 2-10. iSBC® 186/51S Connector P2 Pin Assignments

(Component Size)			(Circuit Size)		
Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	GND	Signal GND	2	GND	Signal GND
3	+5VB	+5V Battery	4	+5VB	+5V Battery
5	-	Not used	6	-	Not used
6	-	Not used	8	-	Not used
9	-	Not used	10	-	Not used
11	-	Not used	12	-	Not used
13	-	Not used	14	-	Not used
15	-	Not used	16	-	Not used
17	-	Not used	18	-	Not used
19	PFIN	Power Fail Interrupt	20	MPRO/	Memory Protect
21	GND	Signal Ground	22	GND	Signal Ground
23	-	Not Used	24	-	Not used
25	-	Not Used	26	-	Not used
27	-	Not Used	28	-	Not used
29	-	Not Used	30	-	Not used
31	-	Not Used	32	BALE	Bus Master Address Latch Enable
33	-	Not used	34	-	Not used
35	-	Not used	36	-	Not used
37	-	Not used	38	AUX RESET/	Reset Switch
39	-	Not used	40	-	Not Used
41	-	Not used	42	-	Not used
43		Not used	44	-	Not used
45	-	Not used	46	-	Not used
47	-	Not used	48	-	Not used
49	-	Not used	50	-	Not used
51	-	Not used	52	-	Not used
53	-	Not used	54	-	Not used
55	ADR16/	Address	56	ADR17/	Address
57	ADR14/	Bus	58	ADR15/	Bus
59	-	Not used	60	-	Not used

Table 2-11. Connector P2 Signal Descriptions

Signal	Functional Description
ADR14/-ADR17/	Address. These 4 address lines are the four most significant address bits in 24-bit addressing.
BALE	Bus Address Latch Enable. Generated by the iSBC 186/51S board to provide auxiliary address latch.
AUX RESET/	Auxiliary Reset. This externally generated signal initiates a power-up sequence.
MPRO/	Memory Protect. This externally generated signal prevents access to the dual port RAM during battery backup operation.
PFIN/	This signal interrupts the board processor when a power failure occurs.

2.14 Serial I/O Interfaces

The serial I/O interfaces are through connectors J1 and J2. The iSBC 186/51S board uses an Intel 8274 Multiprotocol Serial Controller (MPSC) to provide two channels (A and B) of serial input/output. Channel A, through connector J1, can be configured by jumpers as either a RS232C or RS422A/449 interface. In the RS232C configuration either a DTE (Data Terminal Mode) or DCE (Data Set Mode) is possible. In the RS422A/449 configuration only DCE is available. Channel B, connector J2 is RS232C and DCE only. Table 2-12 lists the pin assignments for connector J1 and Table 2-13 lists the pin assignments for connector J2. The iSBC 186/51S board requires a serial I/O cable to be installed at either J1 or J2. See Section 2-28 for a description of the cabling required.

Table 2-12. iSBC® 186/51S Connector J1 Pin Assignments

J1 Pin	RS232 Function	RS232C Pin	J1 Pin	RS449 Function	RS422 Pin
1	Not Used	N/C	1	Not Used	N/C
2	Ground	13	2	Shield	13
3	Not Used	10	3	Not Used	10
4	Not Used	12	4	Terminal Ready (TR(A))	12
5	Transmit Clock (TXC)	24	5	Terminal Ready (TR(B))	24
6	Not Used	11	6	Data Mode (DM(A))	11
7	Not Used	23	7	Data Mode (DM(B))	23
8	Not Used	10	8	Not Used	10
9	Not Used	22	9	Not Used	22
10	Not Used	9	10	Clear to Send (CS(A))	9
11	Not Used	21	11	Clear to Send (CS(B))	21
12	Not Used	8	12	Receive Timing (RT(A))	8
13	Data Terminal Ready (DTR)	20	13	Receive Timing (RT(B))	20
14	Signal Ground (SGND)	7	14	Request to Send (RS(A))	7
15	Not Used	19	15	Request to Send (RS(B))	19
16	Data Set Ready (DSR)	6	16	Receive Data (RD(A))	6
17	Not Used	18	17	Receive Data (RD(B))	18
18	Clear to Send (CTS)	5	18	Not Used	5
19	Receive Clock (RXC)	17	19	Not Used	17
20	Request to Send (RTS)	4	20	Send Data (SD(A))	4
21	Not Used	16	21	Send Data (SD(B))	16
22	Receive Data (RXD)	3	22	Terminal Timing (TT(A))	3
23	Not Used	15	23	Terminal Timing (TT(B))	15
24	Transmit Data (TXD)	2	24	Not Used	2
25	Not Used	14	25	Receive Common (RC)	14
26	Not Used	1	26	Not Used	1

Table 2-13. iSBC® 186/51S Connector J2 Pin Assignments

J2 Pin	RS232 Function	RS232 Pin	J2 Pin	RS232 Function	RS232 Pin
1	Not Used	N/C	14	Signal Ground (SGND)	7
2	Ground	13	15	Not Used	19
3	Not Used	10	16	Data Set Ready (DSR)	6
4	Not Used	12	17	Not Used	18
5	Transmit Clock (TXC)	24	18	Clear to Send (CTS)	5
6	Not Used	11	19	Receive Clock (RXC)	17
7	Not Used	23	20	Request to Send (RTS)	4
8	Not Used	10	21	Not Used	16
9	Not Used	22	22	Receive Data (RXD)	3
10	Not Used	9	23	Not Used	15
11	Not Used	21	24	Transmit Data (TXD)	2
12	Data Carrier Detect (DCD)	8	25	Not Used	14
13	Data Terminal Ready (DTR)	20	26	Not Used	1

2.15 Ethernet Interface

The Ethernet Interface is through connector J3 on the iSBC 186/51S board. The Ethernet Interface consists of an 82586 Local Area Network Controller and a MB502A Adapter Board operating as an interface pair. Connector J3 is tied directly to the MB502A Adapter Board. The MB502A is tied directly to the 82586 Controller. Table 2-14 provides the Ethernet Interface connector pin assignments, Table 2-15 describes the interface signals. The Ethernet connector is tied to the external Ethernet transceiver with the internal transceiver cable. See Section 2.10 for a description of this cable.

Table 2-14. iSBC® 186/51S Ethernet Connector J3 Pin Assignments

Pin	Signal	Description	Pin	Signal	Description
1	TRANSMIT (+)	Transmit (+)	2	TRANSMIT (-)	Transmit (-)
3	RECEIVE (+)	Receive (+)	4	RECEIVE (-)	Receive (-)
5	COLLISION (+)	Collision (+)	6	COLLISION (-)	Collision (-)
7	XCEIVER PWR RTN	Transceiver Power Return	8	XCEIVER PWR RTN	Transceiver Pwr Return
9	XCEIVER PWR	Transceiver Power	10	XCEIVER PWR	Transceiver Power

Table 2-15. iSBC® 186/51S Ethernet Connector J3 Signal Descriptions

Signal	Description
Transmit (+) Transmit (-)	Transmit Data Pair. These two lines generate a differential signal which drives the interface cable with Manchester data.
Receive (+) Receive (-)	Receive Data Pair. This is a differentially driven input to the iSBC 186/51S board where Manchester data is received from the transceiver. The first transition at J3-3 is negative indicating the beginning of a data frame. The last transition should be positive indicating the end of a frame.
Collision (+) Collision (-)	Collision Input Pair. The collisions presence signal is a 10 MHz ± 5% square wave generated by the transceiver input through connector J3 whenever the data frames are superimposed in the coax cable. The first transition at J3-6 is negative to indicate the beginning of the signal and the last transition is positive to indicate the end of a signal.

2.16 iSBX™ Interface

The iSBC 186/51S board has two iSBX (Single Board Expansion) bus connectors (J4 and J5) that allow on-board expansion using iSBX MULTIMODULE boards. Connector J5 cannot be used. The iSBC 186/51S board is fully compatible with the Intel iSBX bus. See the Intel iSBX Bus Specification, 142686. The connector J4 on the iSBC 186/51S board allows installation of one single-wide MULTIMODULE boards.

Table 2-16 provides the pin assignments for connector J4. Table 2-17 provides the pin assignments for connector J5. Connectors J4 and J5 are tied together except for Pins 12, 14, 16, 20, 22, 26, 28, 30, 32 and 34. These ten pins provide similar but not identical signals. The connectors are physically identical.

Table 2-18 provides signal descriptions for the iSBX Bus.

Table 2-16. iSBC® 186/51S Connector J4 Pin Assignments

Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	+12V	+12 Volts	2	-12V	-12 Volts
3	GND	Ground	4	+ 5V	+5 Volts
5	RESET	Reset	6	MCLK	Master Clock
7	A3	Address Bit 3	8	-	-
9	A2	Address Bit 2	10	-	-
11	A1	Address Bit 1	**12**	**SBX2INT1**	**Module 2 Interrupt 1**
13	IOWT/	Input/Output Write	**14**	**SBX2INT0**	**Module 2 Interrupt 0**
15	IORD/	Input/Output Read	**16**	**MWAIT2/**	**Wait State Request 2**
17	GND	Ground	18	+5 V	+5 Volts
19	D7	Data Bit 7	**20**	**SBX2CS1/**	**Module 2 Chip Select 1**
21	D6	Data Bit 6	**22**	**SBX2CS0/**	**Module 2 Chip Select 0**
23	D5	Data Bit 5	24	-	-
25	D4	Data Bit 4	**26**	**TDMA0**	**Terminate DMA0**
27	D3	Data Bit 3	**28**	**OPT1**	**Option 1**
29	D2	Data Bit 2	**30**	**OPT0**	**Option 0**
31	D1	Data Bit 1	**32**	**MDACK2/**	**DMA Acknowledge 2**
33	D0	Data Bit 0	**34**	**MDRQT2**	**DMA Request 2**
35	GND	Ground	36	+ 5V	+5 Volts
37	DE	Data Bit E	38	DF	Data Bit F
39	DC	Data Bit C	40	DD	Data Bit D
41	DA	Data Bit A	42	DB	Data Bit B
43	D8	Data Bit 8	44	D9	Data Bit 9

NOTE: Bold face type indicates pins on J4 not tied to J5.

Table 2-17. iSBC® 186/51S Connector J5 Pin Assignments

Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	+12V	+12 Volts	2	-12V	-12 Volts
3	GND	Ground	4	+ 5V	+5 Volts
5	RESET	Reset	6	MCLK	MULTIMODULE Clock
7	A3	Address Bit 3	8	-	-
9	A2	Address Bit 2	10	-	-
11	A1	Address Bit 1	12	**SBX1INT1**	**Module 1 Interrupt 1**
13	IOWT/	Input/Output Write	14	**SBX1INT0**	**Module 1 Interrupt 0**
15	IORD/	Input/Output Read	16	**MWAIT1/**	**Wait State Request 1**
17	GND	Ground	18	+5 V	+5 Volts
19	D7	Data Bit 7	20	**SBX1CS1/**	**Module 1 Chip Select 1**
21	D6	Data Bit 6	22	**SBX1CS0/**	**Module 1 Chip Select 0**
23	D5	Data Bit 5	24	-	-
25	D4	Data Bit 4	26	**TDMA1**	**Terminate DMA1**
27	D3	Data Bit 3	28	**OPT1**	**Option 1**
29	D2	Data Bit 2	30	**OPT0**	**Option 0**
31	D1	Data Bit 1	32	**MDACK1/**	**DMA Acknowledge 1**
33	D0	Data Bit 0	34	**MDRQT1**	**DMA Request 1**
35	GND	Ground	36	+ 5V	+5 Volts
37	DE	Data Bit E	38	DF	Data Bit F
39	DC	Data Bit C	40	DD	Data Bit D
41	DA	Data Bit A	42	DB	Data Bit B
43	D8	Data Bit 8	44	D9	Data Bit 9

Note: Bold face type indicates pins on J4 not tied to J5.

Table 2-18. iSBX™Bus Signal Descriptions

Signal	Description
IOWT/	MULTIMODULE Write Command. Commands the iSBXMULTIMODULE Board to perform a write operation.
IORD/	MULTIMODULE Read Command. Commands the iSBX MULTIMODULE Board to perform a read operation.
RESET	Reset Signal. Initializes the iSBX MULTIMODULE Board to a known starting state.
SBX2CS0/	MULTIMODULE 2 Chip Select 0. Selects even I/O addresses from 00A0(H) to 00AF(H) for both 8- and 16-bit devices on the J4 connector.
SBX2CS1/	MULTIMODULE 2 Chip Select 1. Selects even I/O addresses from 00B0(H) to 00BF (H) for 8-bit devices on connector J4. Selects odd I/O addresses from 00A0(H) to 00AF(H) for 16-bit devices on connector J4.
SBX1CS0/	MULTIMODULE 1 Chip Select 0. Selects even I/O addresses for both 8- and 16-bit devices on connector J5.

Table 2-18. iSBX™Bus Signal Descriptions (Cont'd.)

Signal	Description
SBX1CS1/	MULTIMODULE 1 Chip Select 1. Selects even I/O addresses from 0090(H) -009F(H) for 8-bit devices on connector J5. Selects even I/O addresses from 0080(H) - 008F(H) for 16-bit devices on connector J5.
A1, A2, A3	Least three bits of the I/O addresses. These three bits provide MULTIMODULE addresses on the iSBX bus. Because A0, the least significant bit, is not supplied to the iSBX connectors, the installed modules respond to even numbered I/O ports. A1, A2, A3 are used in conjunction with the chip select signals (SBX2CS0, SBX2CS1, SBX1CS0, and SBX1CS1) and the command lines.
SBX2INT0 SBX2INT1 SBX1INT0 SBX1INT1	MULTIMODULE Interrupt Lines. Two MULTIMODULE interrupt lines per connector (SBX2INT0 and SBX2INT1 for connector J4 and SBX1INT0 and SBX1INT1 for connector J5) to the interrupt matrix of the iSBC 186/51S board.
MWAIT1/	Wait State Request. MULTIMODULE wait state request to the iSBC 186/51S. Causes the iSBC 186/51S to execute wait states until the MULTIMODULE installed at connector J5 is ready to respond.
MWAIT2/	Wait State Request. Performs the same functions as MWAIT1/ on connector J5 except it is for the MULTIMODULE installed at connector J4.
MCLK	MULTIMODULE Clock. A 10.0 MHz timing reference from the iSBC 186/51S board for the MULTIMODULEs installed at connectors J4 and J5.
MDRQT2	DMA Cycle Request 2. This line is used by the MULTIMODULE at connector J4 to initiate a DMA (Direct Memory Access) cycle on the iSBC 186/51S board.
MDRQT1	DMA Cycle Request 1. This line is used by the MULTIMODULE at connector J5 to initiate a DMA cycle on the iSBC 186/51S board.
MDACK2/	DMA Acknowledge 2. When the DMA controller on the iSBC 186/51S board gains control of the bus in response to the DMA request (MRDQT2) it acknowledges the request back to the MULTIMODULE at connector J4 by generating MDACK2/ and a read or write command.
MDACK1/	DMA Acknowledge 1. When the DMA controller on the iSBC 186/51S board gains control of the bus in response to the DMA request (MDRQT1) it acknowledges the request back to the MULTIMODULE at connector J5 by generating MDACK1/ and a read or write command.
D0-D7 D8-DF	Bidirectional Data Lines. Eight or 16 bidirectional data lines (active high) are used to transmit or receive information to or from the iSBX MULTIMODULE ports. D0 is the least significant bit.

Table 2-18. iSBX™ Bus Signal Descriptions (Cont'd.)

Signal	Description
TDMA1	Terminate DMA1. This signal is used by the MULTIMODULE installed at connector J5 to terminate a DMA cycle.
TDMA0	Terminate DMA2. This signal is used by the MULTIMODULE installed at connector J4 to terminate a DMA cycle.
OPT0-OPT1	Optional Use Lines. These lines may be used for additional interrupt request lines.

2.17 Local Memory Interface

The local memory interface consists of six 28 pin JEDEC sites, configured in pairs, located at U32/U49 (pair 1), U33/U50 (pair 2), and U34/U51 (pair 3). Except for chip select signals (pin 20) each pair of JEDEC sites receive the same input signals. Table 2-19 shows the pin assignments for the JEDEC sites, Table 2-20 provides the DC signal characteristics for the JEDEC site, and Table 2-21 lists the JEDEC site access times. The parameters shown in Table 2-20 are the design parameters for the JEDEC sites. JEDEC site components should not exceed those parameters.

Table 2-19. JEDEC Site Pin Assignments

Pin		Mnemonic	Description
28 Pin Device	24 Pin Device		
1		RDY/, NVEN/, Vpp/, A14	Ready
2		A12	Address Bit 12
3	1	A7	Address Bit 7
4	2	A6	Address Bit 6
5	3	A5	Address Bit 5
6	4	A4	Address Bit 4
7	5	A3	Address Bit 3
8	6	A2	Address Bit 2
9	7	A1	Address Bit 1
10	8	A 0	Address Bit 0
11	9	IO0	Input/Output Data Bit 0
12	10	IO1	Input/Output Data Bit 1
13	11	IO2	Input/Output Data Bit 2
14	12	GND	Ground
15	13	IO3	Input/Output Data Bit 3
16	14	IO4	Input/Output Data Bit 4

Table 2-19. JEDEC Site Pin Assignments (Cont'd.)

Pin		Mnemonic	Description
28 Pin Device	24 Pin Device		
17	15	IO5	Input/Output Data Bit 5
18	16	IO6	Input/Output Data Bit 6
19	17	IO7	Input/Output Data Bit 7
20	18	CE/	Chip Enable
21	19	A10	Address Bit 10
22	20	OE	Output Enable
23	21	AB1, (see Note)	Address Bit 11 (see Note) Vpp
24	22	A9	Address Bit 9
25	23	A8	Address Bit 8
26	24	Vcc, A13	Vcc, Address Bit 13
27		WE/,A14	Write Enable, Address Bit 14
28		Vcc	Vcc

NOTE: Ready, Non-Volatile RAM Enable, Vpp, Address Bit 14

Table 2-20. 28-Pin JEDEC Site DC Signal Characteristics

Parameter	Min	Max	Units
V_{IL}		0.8	V
V_{IH}	2.0		V
I_{IL}		$\pm$10	µA
I_{IH}		$\pm$10	µA
V_{OL}		0.45	V
V_{OH}	2.4		V
C_{IN}		6	pfd
C_{IN} (Data)		12	pfd

Table 2-21. JEDEC Site Access Times

JEDEC Sites	Remarks
U32 / U49	0 - Wait Access, 270 ns 1 - Wait Access, 435 ns
U33 / U50	0 - Wait Access, 270 ns 1 - Wait Access, 435 ns
U34 / U51	0 - Wait Access, 308 ns 1 - Wait Access, 473 ns

2.18 iSBC® 186/51S Board Set-Up

The iSBC 186/51S board provides a variety of jumper selectable options to allow user configuration of the board according to the functions performed on the board. Sections 2-19 through 2-25 describe the selectable options and the required jumper configurations. Table 2-22 lists the jumpers on the iSBC 186/51S board and shows in which of the following tables their function is described. Table 2-22 also locates the jumpers on the schematic diagram of the board shown in Section 5.

2.19 Processor Section Set-Up

The processor section consists of the 80186 microprocessor and its support circuitry. Because the 80186 processor includes a CPU, three timers, two DMA channels and a clock generator the user has several available options.

DMA requests to the two DMA channels of the 80186 can come from one of six sources:

1. 8274 Channel A Transmit Request
2. 8274 Channel A Receive Request
3. 8274 Channel B Transmit Request
4. 8274 Channel B Receive Request
5. SBX 1 DMA Request
6. SBX 2 DMA Request

Any one of the six sources can be connected to either DMA channel, the stake pins are laid out to provide easy "push on" connection for the request sources.

Table 2-22. iSBC® 186/51S Jumpers, Numerical Reference and Default Jumper Summation

Stake Pins	Table Ref.	Sch. Ref. Fig 5-3 Sheet	Stake Pins	Table Ref.	Sch. Ref. Fig 5-3 Sheet	Stake Pins	Table Ref.	Sch. Ref. Fig 5-3 Sheet
E1*	2-24	8	E46*	2-26	3	E91*	2-5	9
E2*	2-24	8	E47*	2-26	3	E92*	2-5	9
E3	2-24	8	E48*	2-26	3	E93*	2-5	9
E4*	2-24	8	E49*	2-26	3	E94*	2-5	9
E5*	2-24	8	E50*	2-26	3	E95**	Not Used	9
E6	2-24	8	E51*	2-26	3	E96**	Not Used	9
E7*	2-24	8	E52*	2-26	3	E97**	Not Used	9
E8*	2-24	8	E53*	2-26	3	E98	2-5	9
E9*	2-24	8	E54*	2-26	3	E99**	Not Used	9
E10*	2-24	8	E55*	2-26	3	E100**	Not Used	9
E11	2-24	8	E56*	2-26	3	E101**	Not Used	9
E12*	2-23	2	E57*	2-26	3	E102**	Not Used	9
E13	2-26	3	E58*	2-26	3	E103	2- 5	9
E14	2-26	3	E59	2-24	11	E104	2- 5	9
E15*	2-23	2	E60	2-24	11	E105*	2- 5	9
E16	2-26	3	E61	2-24	11	E106**	Not Used	9
E17	2-26	3	E62*	2-24	11	E107*	2- 5	9
E18	2-26	3	E63*	2-24	11	E108	2- 5	9
E19	2-26	3	E64	2-28	12	E109*	2- 5	9
E20	2-26	3	E65	2-28	12	E110*	2- 5	9
E21	2-23	2	E66	2-28	12	E111*	2- 5	9
E22	2-26	3	E67*	2-23	2	E112*	2- 5	9
E23	2-26	3	E68*	Sect. 2-27	4	E113	2- 5	9
E24*	2-23	2	E69*	Sect. 2-27	4	E114*	2- 5	9
E25	2-23	2	E70*	2-23	2	E115	2- 5	9
E26	2-26	3	E71	2-23	2	E116*	2- 5	9
E27*	2-23	2	E72	2-23	2	E117	2- 5	9
E28*	2-23	2	E73	2-28	12	E118	2- 5	9
E29*	2-23	2	E74	2-28	12	E119	2- 5	9
E30*	2-23	10	E75*	2-23	2	E120	2- 5	9
E31*	2-23	10	E76	2-23	2	E121	2-25	10
E32*	Sect. 2-27	3	E77*	2-23	3	E122	2-25	10
E33*	Sect. 2-27	3	E78	2-23	2	E123	2-25	10
E34*	2-23	3	E79*	2-23	2	E124	2-25	10
E35*	2-23	3	E80	2-23	2	E125	2-25	10
E36	2-26	3	E81*	2-23	3	E126	2-25	10
E37	2-26	3	E82	2-26	3	E127	2-25	10
E38	2-26	3	E83	2-26	3	E128	2-25	10
E39	2-26	3	E84	2-28	12	E129	2-25	10
E40	2-26	3	E85	2-28	12	E130*	2-31	10
E41	2-26	3	E86	2-28	12	E131*	2-31	4
E42	2-26	3	E87	Sect. 2-27	2	E132	2-31	4
E43*	2-26	3	E88*	Sect. 2-27	2	E133	2-25	10
E44*	2-26	3	E89*	Sect. 2-27	2	E134	2-25	10
E45*	2-26	3	E90	2-23	3	E135*	2- 5	9

Table 2-22. iSBC® 186/51S Jumpers, Numerical Reference and Default Jumper Summation (Cont'd.)

Stake Pins	Table Reference	Schematic Reference Fig 5-3 Sheet	Stake Pins	Table Reference	Schematic Reference Fig 5-3 Sheet	Stake Pins	Table Reference	Schematic Reference Fig 5-3 Sheet
E136*	2-5	9	E164	2-31	2	E192	2-27	8
E137**	Not Used	9	E165	2-31	2	E193	2-32	3
E138	2-5	9	E166	2-30	5	E194*	2-26	3
E139**	Not Used	9	E167	2-30	5	E195	2-26	3
E140**	Not Used	9	E168*	2-31	4	E196	2-30	5
E141	2-5	9	E169	2-31	4	E197	2-29	5
E142*	2-5	9	E170	2-31	4	E198	2-29	5
E143	2-5	9	E171	2-31	4	E199*	2-4	8
E144*	2-5	9	E172	2-30	4	E200	2-27	8
E145*	2-5	9	E173	2-30	5	E201	2-29	5
E146	2-5	9	E174*	2-31	4	E202	2-29	5
E147*	2-5	9	E175*	2-31	4	E203*	2-4	8
E148	2-5	9	E176	2-26	3	E204	2-26	8
E149	2-5	9	E177	2-26	3	E205	2-32	10
E150	2-29	5	E178	2-26	3	E206	2-32	10
E151	2-29	5	E179	2-26	3	E207	2-32	10
E152*	2-29	5	E180	2-29	5	E208	2-32	10
E153	2-29	5	E181	2-30	5	E209*	2-32	10
E154	2-29	5	E182	2-30	5	E210	2-32	10
E155*	2-29	5	E183*	2-31	4	E211	2-32	10
E156	2-29	5	E184	2-26	3	E212	2-32	10
E157	2-29	5	E185*	2-26	3	E213*	2-32	10
E158	2-29	5	E186	2-26	3	E214*	Sect. 2.25	7
E159	2-29	5	E187	2-26	3	E215*	Sect. 2.25	7
E160	2-29	5	E188	2-29	5	E216	Sect. 2.25	7
E161	2-29	5	E189	2-29	5	E217*	Batt. Sel	1
E162	2-31	2	E190	2-29	5	E218*	Batt. Sel	1
E163	2-31	2	E191	2-4	8	E219*	Batt. Sel	1
						E220*	Batt. Sel	1

Default Jumper Summation

Jumper	Remarks	Table Reference	Schematic Reference Fig 5-3 Sheet
E1 to E2	Channel B Interrupt or Polled	2-24	8
E4 to E5	Channel A TX Clock to Timer 0	2-24	8
E7 to E8	Channel B TX Clock to Timer 1	2-24	8
E9 to E10	Channel B RX Clock to TX Clock	2-24	8
E12 to E15	Time Out Non-Maskable Interrupt NMI (80186)	2-23	2
E24 to E27	8274 Channel A Transmit Request	2-23	2
E28 to E29	16M Clock to 80186 (12MHz)	2-23	2
E30 to E31	Test Jumper	Sect. 2.27	10
E32 to E33	Test Jumper	Sect. 2.27	3
E34 to E35	Enable Bus Time Out	2-23	3
E43 to E47	8274 Interrupt (Source for 80130A) 8274 Interrupt (Destination IR3 of 80130A)	2-26	3

Table 2-22. iSBC® 186/51S Jumpers, Numerical Reference and Default Jumper Summation (Cont'd.)

Default Jumper Summation			
Jumper	Remarks	Table Reference	Schematic Reference Fig 5-3 Sheet
E44 to E48	80130A SYSTICK (Source for 80130A) / 80130A SYSTICK 8274 Interrupt (Destination IR2 of 80130A)	2-26	3
E45 to E49	SBX2 Interrupt 0 (Source for 80130A)/ SBX2 Interrupt 0 (Destination IR1 of 80130A)	2-26	3
E46 to E50	82586 Interrupt (Source)/82586 Interrupt (Destination IR0 of 80130A)	2-26	3
E51 to E55	Flag Interrupt (Source)/Flag Interrupt (Destination IR7 of 80130A)	2-26	3
E52 to E56	SBX2 Interrupt 1 (Source)/SBX2 Interrupt (Destination IR6 of 80130A)	2-26	3
E53 to E57	MULTIBUS Interrupt (Source for 80130A)/ MULTIBUS Interrupt (Destination IR5 of 80130A)	2-26	3
E54 to E58	Slave Interrupt (Source for 80130A)/Slave Interrupt (Destination IR4 0f 80130A)	2-26	3
E62 to E63	Channel A RX Clock to External Source.	2-24	11
E67 to E70	8274 Channel A Receive Request	2-23	2
E68 to E69	Factory Test Jumper	Sect. 2.27	4
E75 to E79	Disable Test Pin	2-23	2
E77 to E81	Enable 1 PROM Wait State.	2-23	3
E88 to E89	Factory Test Jumper	Sect. 2-27	2
E91 to E92	Local Memory Device Selection Jumper	2-5	9
E93 to E94	Local Memory Device Selection Jumper	2-5	9
E105 to E109	Local Memory Device Selection Jumper	2-5	9
E110 to E114	Local Memory Device Selection Jumper	2-5	9
E112 to E116	Local Memory Device Selection Jumper	2-5	9
E130 to E131	Enables Lock Line to MULTIBUS Interface P1-25	2-31	4
E135 to E136	Local Memory Device Selection Jumper	2-5	9
E142 to E144	Local Memory Device Selection Jumper	2-5	9
E145 to E147	Local Memory Device Selection Jumper	2-5	9
E152 to E155	Dual Port RAM MULTIBUS Address Selection Jumper	2-29	5
E168 to E174	Enables BPRO/ to the MULTIBUS Interface P1-16	2-31	4
E175 to E183	Enables Common Bus Request (CBRQ) line to MULTIBUS Interface P1-29.	2-31	4
E185 to E194	MULTIBUS Interrupt 5 (Source)/Interrupt Inverter 1 Input (Source).		3
E199 to E203	JEDEC Size Selection Jumper	2-4	8
E214 to E215	REFRQ Select	Sect.2-25	7
E217 to E219	Battery Select	-	1
E218 to E220	Battery Select	-	1

NOTE: * Indicates default pins, actual pairing are shown under "Default Jumper Summation."

** Use depends on type of memory device installed.

Two of the three timers on the 80186 can count pulses on timing input lines TMRIN1 and TMRIN2. Since these timers are normally used for baud rates to the 8274 controller, the TMRIN1 and TMRIN2 input lines normally would not be used. The lines are, however, brought out to stake pins for user use.

The 80186 test pin which is sampled by the test instruction is tied to ground by jumper E75-E79. An external signal can be connected to E75 by removing the jumper. The 80186 processor will then wait for the external signal to occur before proceeding.

Two jumper sets, E12-E15 and E34-E35, enable time outs. If a time out is enabled, a time out will occur whenever the processor is inactive longer than the timeout time. This situation can be caused by the processor accessing non-existent MULTIBUS resources, not being able to get on the MULTIBUS interface or if the processor is locked out of the dual port RAM. Because it is desirable that the processor knows a time out has occurred the timeout is jumpered to the NMI input of the processor via the E12-E15 jumper. Table 2-23 lists the 80186 processor section jumpers. A single stake pin indication in Table 2-23 means that signal is available to the user at that location.

2.20 Local Memory Options

The local memory options are discussed in Section 2-9. The type of memory devices installed and their capacities determine the installation of various jumpers. Table 2-4 lists the capacity determined jumpers and Table 2-5 lists the device type determined jumpers.

Table 2-23. Processor Section Jumpers

Jumper	Function
E12 - E15*	Time Out Non-Maskable Interrupt (NMI)
E21 - E24	SBX1 DMA Req
E24 - E 27*	8274 Channel A Transmit Request
E25	8274 Channel B Transmit Request
E28 - E29	16 M CLK
E30 - E31*	Enable Bus Time Out
E34 - E35*	Enable Bus Time Out
E67 - E70*	8274 Channel A Receive Request
E70 - E72	SBX2 DMA Request
E71	8274 Channel B Receive Request
E75 - E79*	Disable Test Pin
E76	Timer 1 Input
E77 - E81*	Enable 1 PROM Wait State
E78	TMROUT 1 Output from 80186
E80	Timer 0 Input
E90	Delay Output of 80130A

NOTE: * Indicates default connection.

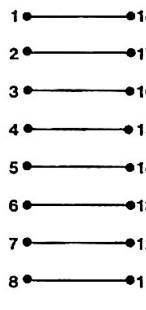
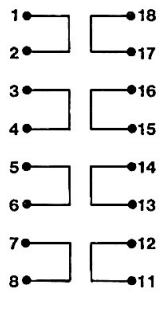
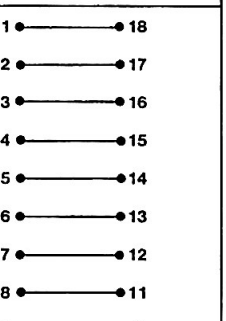
2.21 Serial Interface Options

The iSBC 186/51S board uses an 8274 Multi-Protocol Serial Controller at U22 to provide two channels (A and B) of serial I/O. Channel A can be configured to have either RS232C, DCE or DTE interface or an RS422A/449/ DCE interface. In the RS422A/449 configuration the drivers can be three-stated to allow multi-drop networks. Channel B can have only RS232C and DCE only. Table 2-24 shows the options and the options and their associated jumpers for the two general purpose serial channels.

In addition to the jumpers listed in Table 2-24, two headers at U18 and U19 must be connected as shown in Figure 2-3 for the desired configuration of the serial channels. Table 2-3 gives the header part number.

2.22 Parallel I/O Options

There are four general purpose inputs which can be read by the iSBC 186/51S board's on-board processor. These four jumper selectable inputs can be used for a variety of purposes such as indicating system configuration and timeouts. Table 2-25 lists the jumper combinations that determine the general purpose inputs.

RS232C/DCE	RS232C/DTE	RS422A/449
 HEADER AT XU18*	 HEADER AT XU18**	NOT INSTALLED HEADER AT XU18**
NOT INSTALLED HEADER AT XU19	NOT INSTALLED HEADER AT XU19	 HEADER AT XU19
RP2 — NOT INSTALLED RP3 — 2K RP4 — 2K INSTALLED BACKWARDS, PIN 1 INTO PIN 6	RP2 — NOT INSTALLED RP3 — NOT INSTALLED RP4 — NOT INSTALLED	RP2 — INSTALLED FOR LAST MULTIDROP SLAVE OR POINT TO POINT. RP3 AND RP4 — INSTALLED FOR MULTIDROP MASTER.
3487 DEVICE AT XU3 NOT INSTALLED	3487 DEVICE AT XU3 NOT INSTALLED	3487 DEVICE AT XU3 INSTALLED

* INTEL FURNISHED
** USER FURNISHED

Figure 2-3. Channel A RS422A/449 to RS232 C Conversion

Table 2-24. Serial Interface Option Jumpers

Jumper	Function	Jumper	Function
E1 to E2*	Channel B Interrupt	E9 to E10*	Channel B RX Clock to TX Clock.
E3 to E4	Channel A TX Clock to External Source. Use DTE as source	E10 to E11	Channel B RX Clock to External Source. Use DTE as source.
E4 to E5*	Channel A TX Clock to Timer 0	E59 to E60	Controls RS422A Three-State with DTR. DTR On = enable.
E6 to E7	Channel B TX Clock to External Source. Use DTE as source.	E61 to E62	Channel A RX Clock to TX Clock
E7 to E8*	Channel B TX Clock to Timer 1	E62 to E63*	Channel A RX Clock to External Source. Use DTE as source.

Table 2-25. Parallel I/O Jumpers

Jumper	Remarks
E121 to E122	This jumper, when installed, provides a means to indicate if a timeout has occurred while the iSBC 186/51S was waiting for the MULTIBUS. See Sections 4.2.13 and 4.3.12.
E124 to E125	This jumper, when installed, provides a means to indicate if a software reset has occurred. See Section 4.2.13 and 9.3.12.
E126 to E127	This jumper, when installed, provides a means to indicate if a timeout has occurred. See Sections 4.2.13 and 9.3.12.
E132 to E133	This jumper, when installed, provides a means to indicate if the iSBC 304 Memory Expansion MULTIMODULE is installed. See Section 4.2.13 and 4.3.12. E123, E128, E129 and E134 are ground pins.

2.23 Interrupt Control Options

There are two interrupt controllers on the iSBC 186/51S board. One controller is integrated into the 80186 processor, the other is a 80130A device. The 80186 must be initialized so the programmable interrrupt controller on the 80186 is slaved to the 80130A. The iSBC 186/51S board does not support MULTIBUS vectored interrupts. Table 2-26 lists the interrupt sources and destinations, and their associated stake pins.

Table 2-26. Interrupt Control Stake Pins

Stake Pin	Function	Stake Pin	Function
E13	Interrupt Inverter 6 Input	E50*	82586 Interrupt (Input to IR0 of 80130A)
E14	Interrupt Inverter 6 Output	E51	Flag Interrupt Output
E16	Interrupt Inverter 3 Output	E52*	SBX2 Interrupt 1 Output
E17	Interrupt Inverter 3 Input	E53*	MULTIBUS Interrupts 0 through 7, inverted, only one can be selected, (Output for 80130A)
E18	Latched Interrupt (Output)	E54*	Slave Interrupt (Output for 80130A)
E19	Interrupt Inverter 4 Output	E55*	Flag Interrupt (Input to IR7 of 80130A)
E20	Interrupt Inverter 4 Input	E56*	SBX2 Interrupt 1 (Input to IR6)
E22	Interrupt Inverter 5 Output	E57*	MULTIBUS Interrupt 0 through 7, inverted, only one can be selected, (Input to IR5 of 80130A)
E23	Interrupt Inverter 5 Input	E58*	Slave Interrupt (Input to IR4 of 80130A)
E26	Power Failure Interrupt (Output)	E82	MULTIBUS Interrupt Output
E36	Interrupt NOR Gate Input 1	E83	Latched Interrupt Input
E37	SBX1 Interrupt 0 (Output)	E176	Bus Flag Interrupt Output
E38	SBX1 Interrupt 1 (Output)	E177	MULTIBUS Interrupt 0 Input/Output
E39	Interrupt NOR Gate Input 2	E178	MULTIBUS Interrupt 2 Input/Output
E40	Interrupt NOR Gate Output	E179	MULTIBUS Interrupt 4 Input/Output
E41	Interrupt Inverter 2 Output	E184	MULTIBUS Interrupt 7(Input/Output)
E42	Ground (Output)	E185*	MULTIBUS Interrupt 5 (Input/Output)
E43*	8274 Interrupt (Output)	E186	MULTIBUS Interrupt 3 (Input/Output)
E44*	80130A SYSTICK Output	E187	MULTIBUS Interrupt 1 (Input/Output)
E45*	SBX2 Interrupt 0 Output	E193	MULTIBUS Interrupt 6 (Input/Output)
E46*	82586 Interrupt Output	E194*	Interrupt Inverter 1 Input (Input)
E47*	8274 Interrupt (Input to IR3 of 80130A)	E195	Interrupt Inverter 2 Input (Input/Output)
E48*	80130A SYSTICK 8274 Interrupt (Input to IR2 of 80130A)		
E49*	SBX2 Interrupt 0 (Input to IR1 of 80130A)		

NOTE: * Indicates default pin, See Table 2-22 for Default connections

2.24 iSBX™ Interface Options and Jumpers

Two 8/16 bit iSBX interface connectors are provided for local I/O expansion. Since the iSBC 186/51S board does not support the iSBX MULTIMODULE present signal (MPST/), the iSBX I/O address space is always dedicated to the iSBX interfaces. Jumpers are provided to select an 8- or 16-bit iSBX module address as shown in Table 2-27.

Three options pins OPT0, OPT1 and TDMA are associated with the iSBX interface. OPT0 and OPT1 are two reserved lines that are connected to two stake pins E84 and E85 (for iSBX Interface 1, connector J5) and E65 and E64 (for iSBX Interface 2, connector J4) on the iSBC 186/51S. These lines are for unique requirements where a user needs a base board signal on the iSBX MULTIMODULE board and is willing to put a potentially long wire on the iSBC 186/51S board to connect it.

TDMA is an active high output signal from the iSBX MULTIMODULE board to the iSBC 186/51S board. TDMA can be used by the iSBX MULTIMODULE board to terminate DMA activity on the iSBC 186/51S. Table 2-28 summarizes the iSBX Interface options and their associated stake pins.

Table 2-27. iSBX™ Bus Size Selection Jumpers

Jumper	Function
E192 to E200 - Out E200to E204 - N/A	iSBX1 Interface at J5 set at 8-bit module address
E192 to E200 - Installed E200 to E204 - N/A	iSBX1 Interface at J5 set at 16-bit module address
E192 to E200 - N/A E200 to E204 - Out	iSBX2 Interface at J4 set at 8-bit module address
E192 to E200 - N/A E200 to E204 - Installed	iSBX2 Interface at J4 set at 16-bit module address

Table 2-28. iSBX™ Interface Options Jumpers

Stake Pin	Function	Stake Pin	Function
E64	iSBX2 Interface, Option 1 Line	E74	MDACK2/
E65	iSBX2 Interface, Option 0 Line	E84	iSBX2 Interface, Option 0 Line
E66	iSBX2 Interface, TDMA2	E85	iSBX1 Interface, Option 1 Line
E73	MDACK1/	E86	iSBX1 Interface, TDMA1

2.25 Dual Port Memory Jumpers

The dual port memory consists of an array of sixteen 2164 dynamic RAMs and an 8203 Dynamic RAM controller. The dual port memory size is 128K Bytes expandable to 256K Bytes with the installation of an iSBC 304 Memory Expansion MULTIMODULE.

As seen from the iSBC 186/51S board's on-board processor the dual-port memory always exists at the bottom of memory (the lowest address).

As seen from the MULTIBUS interface, the dual port RAM can be mapped anywhere in the 16M Byte address space. The amount of dual port RAM visible to the MULTIBUS can be 0.0, 0.25, 0.5, 0.75 or all of the dual port RAM. When less than all of the dual-port RAM is visible to the MULTIBUS, the visible part maps to the upper portion of the dual port as seen by the on-board processor.

To configure the address and size of the dual port RAM, set the address using the jumpers in Table 2-29. After setting the address, set the size of the memory to be visible to the MULTIBUS using the jumpers shown in Table 2-30.

In addition to the stake pins listed in Tables 2-29 and 2-30, stake pins E216, E215, and E214 determine the state of the REFRQ pin of the 8203 Dynamic Controller in the dual port RAM. When E216 is tied to E215 the MULTIBUS is allowed to provide an off-board refresh request. With E215 tied to E214 the REFRQ input to the controller is grounded and the refresh operation to the RAM array is performed automatically by the controller. This is the default configuration.

Table 2-29. Dual Port RAM MULTIBUS® Address Selection

	E180 to E188	E150 to E153	E158 to E161	E157 to E160	E151 to E154	E152 to E155	E156 to E159	E190 to E189	E198 to E197	E202 to E201
Megabyte Page	Select the 1M Byte Page (16 Possible)									
None (20 Bit Addr)	Out	X	X	X	X	N/A	N/A	N/A	N/A	N/A
0XXXXXH	In	Out	Out	Out	Out	N/A	N/A	N/A	N/A	N/A
1XXXXXH	In	Out	Out	Out	In	N/A	N/A	N/A	N/A	N/A
2XXXXXH	In	Out	Out	In	Out	N/A	N/A	N/A	N/A	N/A
3XXXXXH	In	Out	Out	In	In	N/A	N/A	N/A	N/A	N/A
4XXXXXH	In	Out	In	Out	Out	N/A	N/A	N/A	N/A	N/A
5XXXXXH	In	Out	In	Out	In	N/A	N/A	N/A	N/A	N/A
6XXXXXH	In	Out	In	In	Out	N/A	N/A	N/A	N/A	N/A
7XXXXXH	In	Out	In	In	In	N/A	N/A	N/A	N/A	N/A
8XXXXXH	In	In	Out	Out	Out	N/A	N/A	N/A	N/A	N/A
9XXXXXH	In	In	Out	Out	In	N/A	N/A	N/A	N/A	N/A
AXXXXXH	In	In	Out	In	Out	N/A	N/A	N/A	N/A	N/A
BXXXXXH	In	In	Out	In	In	N/A	N/A	N/A	N/A	N/A
CXXXXXH	In	In	In	Out	Out	N/A	N/A	N/A	N/A	N/A
DXXXXXH	In	In	In	Out	In	N/A	N/A	N/A	N/A	N/A
EXXXXXH	In	In	In	In	Out	N/A	N/A	N/A	N/A	N/A
FXXXXXH	In	In	In	In	In	N/A	N/A	N/A	N/A	N/A
256K Segment	Select 256K Segment within 1M Byte Page (4 Possible)									
X00000-X3FFFF	N/A	N/A	N/A	N/A	N/A	Out	Out	N/A	N/A	N/A
X40000-X7FFFF	N/A	N/A	N/A	N/A	N/A	Out	In	N/A	N/A	N/A
X80000-XBFFFF	N/A	N/A	N/A	N/A	N/A	In	Out	N/A	N/A	N/A
XC0000-XFFFFF	N/A	N/A	N/A	N/A	N/A	In	In	N/A	N/A	N/A
Top Address	Select Top MULTIBUS Dual Port Address (8 Possible Each Segment)									
X07FFF	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	In
X0FFFF	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	In	Out
X17FFF	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	Out	In
X1FFFF	N/A	N/A	N/A	N/A	N/A	N/A	N/A	In	Out	Out
X27FFF	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Out	In	In
X2FFFF	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Out	In	Out
X37FFF	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Out	Out	In
X3FFFF	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Out	Out	Out

X = Don't Care

Table 2-30. Dual Port Size Selection

Size	E188 - E196	E166 - E167*	E182 - E181	E172 - E173
0K	In	X	X	X
32K	Out	Out	In	In
64K	Out	Out	In	Out
96K	Out	Out	Out	In
128K	Out	Out	Out	Out
64K	Out	In	In	In
128K	Out	In	In	Out
192K	Out	In	Out	In
256K	Out	In	Out	Out

NOTE: X means don't care.
* iSBC 304 select

2.26 MULTIBUS® Interface Jumpers

The iSBC 186/51S board can be a MULTIBUS master in a multimaster system. In addition to all the required MULTIBUS master signals, two additional signals LOCK and CBRQ/ (Common Bus Request) are supported. Table 2-31 lists the MULTIBUS option jumpers.

Table 2-31. MULTIBUS® Interface Option Jumpers

Jumper	Function
E130 - E131*	Enables LOCK/ line to MULTIBUS Interface P1-25.
E162 - E163	Supplies CCLK/ from ESI U31 to MULTIBUS Interface P1-31.
E164 - E165	Supplies BCLK/ from ESI U32 to MULTIBUS Interface P1-13.
E168 - E174*	Enables BPRO/ to the MULTIBUS Interface P1-16.
E169 - E175	Grounds Common Bus Request (CBRQ/) line to the 8289 Bus Arbiter U58.
E170 - E171	Grounds ANY RQST line to 8289 Bus Arbiter U58.
E175 - E183*	Enables Common Bus Request (CBRQ/) line to MULTIBUS Interface P1-29.

NOTE: *Indicates default connection.

The iSBC 186/51S board has a mechanism called the flag byte that signals interrupts between the iSBC 186/51S board's on-board 80186 processor and a MULTIBUS processor. The flag byte is I/O mapped from both the on-board processor's vantage point and the MULTIBUS. PALs U83 and U11 in the Flag Byte Logic generates two

jumper selectable address select signals as the result of processing address bits ADR0 through ADRF, along with three other jumper selectable inputs. The address bits and the jumpered inputs determine at what addresses the flag byte interrupt will be generated. Table 2-32 shows the MULTIBUS I/O address selection jumpers and selected addresses.

Table 2-32. MULTIBUS® I/O Address Selection

MULTIBUS Address Select Jumpers			Selected Address (Hex)	
E210 - E206	E211 - E207	E212 - E208	16 Bit Mode (E213 - E209)*	8 Bit Mode (E209 - E205)
In	In	In	08A4	A4
In	In	Out	08A5	A5
In	Out	In	08A6	A6
In	Out	Out	08A7	A7
Out	In	In	09A4	A4
Out	In	Out	09A5	A5
Out	Out	In	09A6	A6
Out*	Out*	Out*	09A7	A7

NOTE: * Indicates default connection

2.27 Test Jumpers

The jumper connections listed below are factory test jumpers. The jumpers should not be removed for normal board operation.

Jumper	Schematic Location
E31 to E30*	Schematic (Figure 5-3), Sheet 10
E32 to E33*	Schematic (Figure 5-3), Sheet 3
E68 to E69*	Schematic (Figure 5-3), Sheet 4

* Indicates default connection.

NOTE

E88 (82586 CTS) is connected to E89 (Gnd) in the default condition. E88 is connected to E87 if a "watchdog" timer is being used.

2.28 Serial I/O Cabling Requirements

The iSBC 186/51S board requires a serial I/O cable and connectors for its J1 and J2 connectors. The J1 interface can be either a RS232C or a RS422 interface. Headers installed on the iSBC 186/51S board (see Figure 2-3) determine which interface configuration is applicable. The J2 interface is an RS232C interface. Either connector/interface combination uses the same cabling.

Table 2-12 lists the pin assignments for connector J1, Table 2-13 does the same for connector J2. Figure 2-4 shows a wiring diagram for a serial I/O cable. Figure 2-5 shows the installation of the cable. When assembling the cable please note that connection is not point to point, that is, Pin 2 on the ISBC 186/51S side of the cable is not connected to pin 2 of the connector at the other end of the cable.

When installing the cable on connector J1 or J2 of the iSBC 186/51S board the arrow on the board connector will align with the arrow on the cable connector (P/N 3399-6000 or P/N 88376-3).

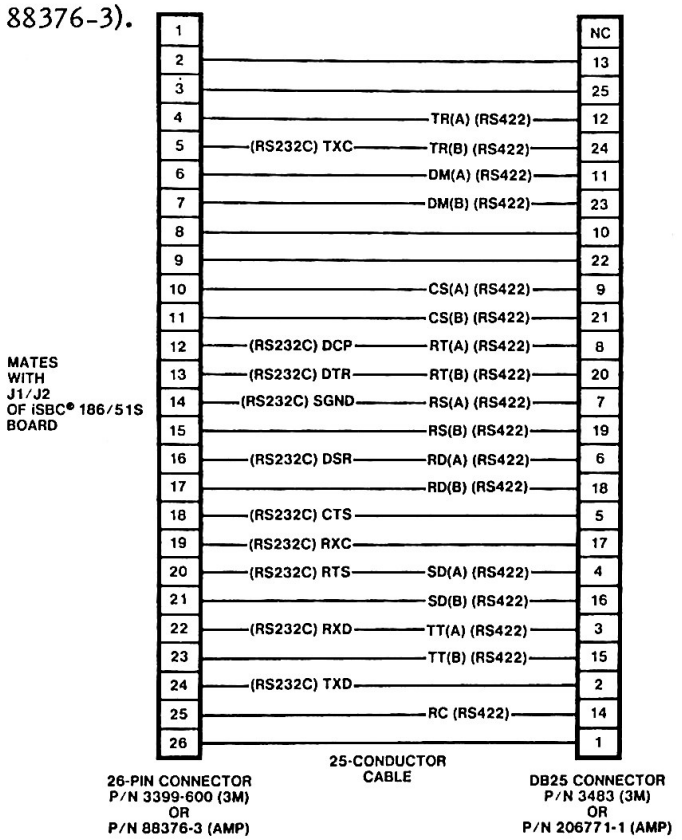


Figure 2-4. Serial I/O Cable Wiring Diagram

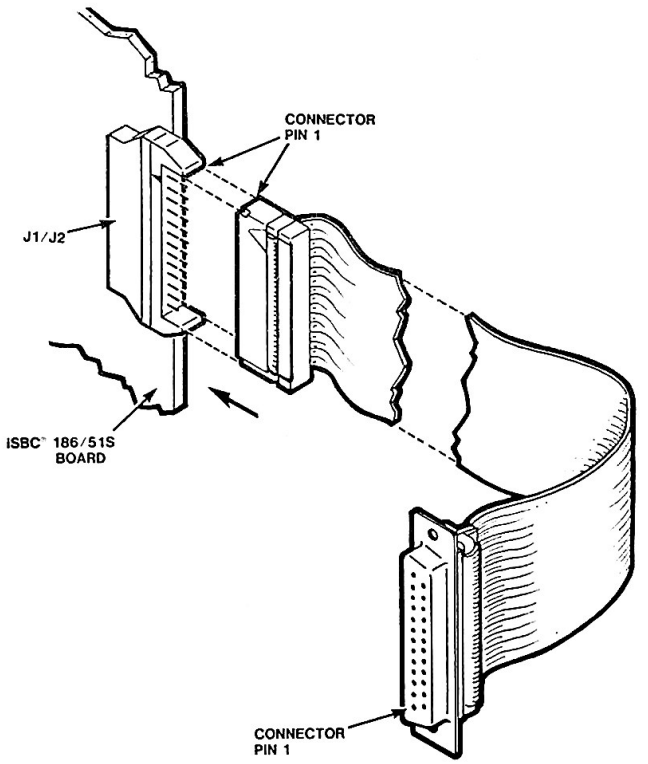


Figure 2-5. Serial I/O Cable Installation Drawing

CHAPTER 3. PROGRAMMING INFORMATION

3.1 Introduction

The iSBC 186/51S board contains several programmable devices. This chapter provides the necessary programming information for the devices and provides typical programming examples for each. Memory and I/O port addresses are provided in tabular form.

3.2 Programming Considerations

This paragraph describes how the iSBC 186/51S board is programmed. Address space assignments and bit assignments are provided. To facilitate the discussion the board is broken into the following blocks:

1. Memory Addressing
2. Processor Programming
   a. Chip Select and Ready Initialization
   b. 16M Byte Master Initialization
   c. 80186 Peripheral Initialization
3. Ethernet Controller
4. Local Memory
5. Local I/O
6. Flag Byte Signalling

3.2.1 MEMORY ADDRESSING

The addresses used by the 80186 local CPU, and the 82586 Local Communication Controller (LCC) in accessing the local memory and the dual port RAM are referred to in the text as local addresses, and those used by the MULTIBUS devices in accessing the dual port RAM are referred to as the MULTIBUS addresses. The relationship between the addresses is shown in Figure 3-1 and Table 3-1.

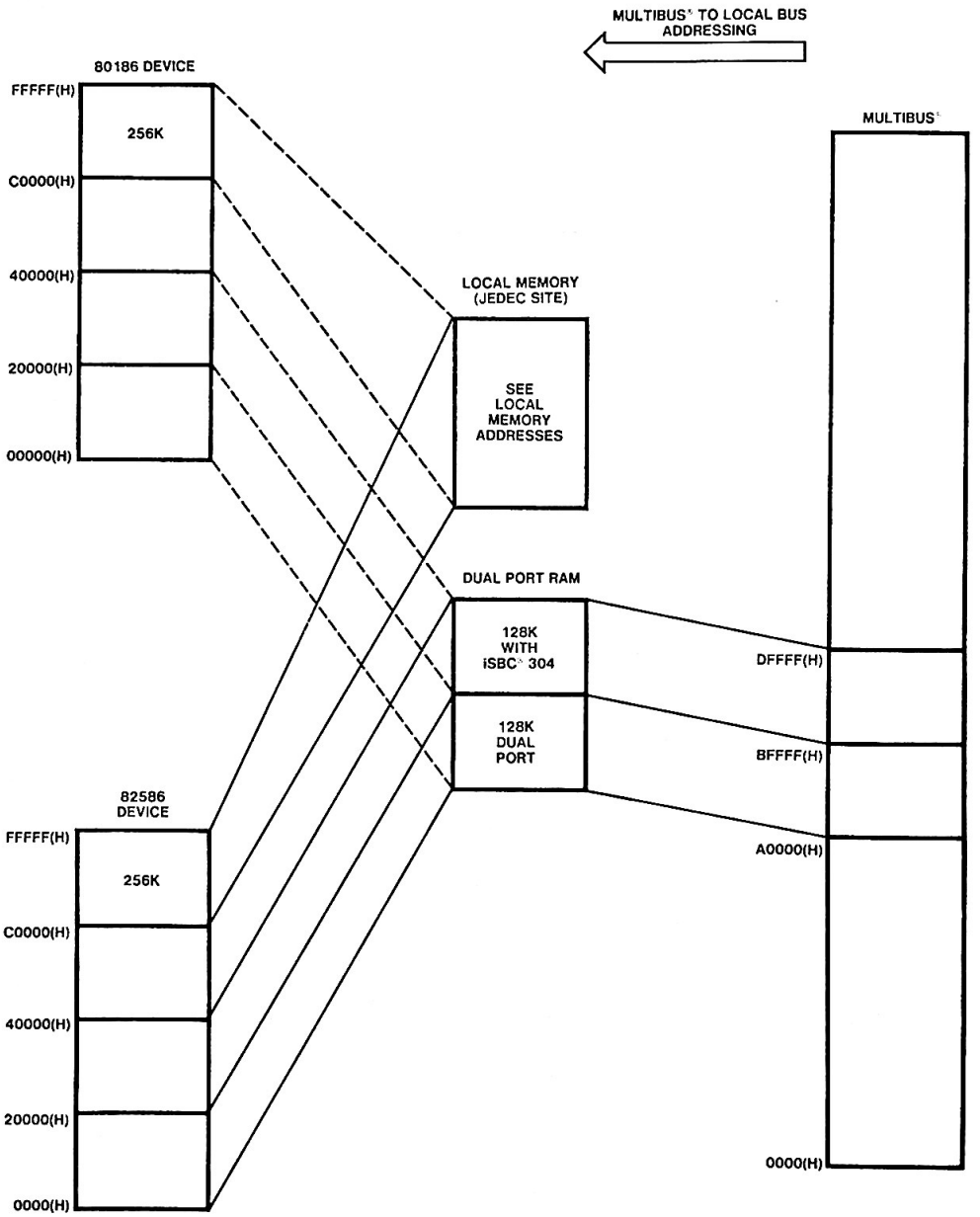


Figure 3-1. iSBC® 186/51S Board Memory Map (Sheet 1 of 4)

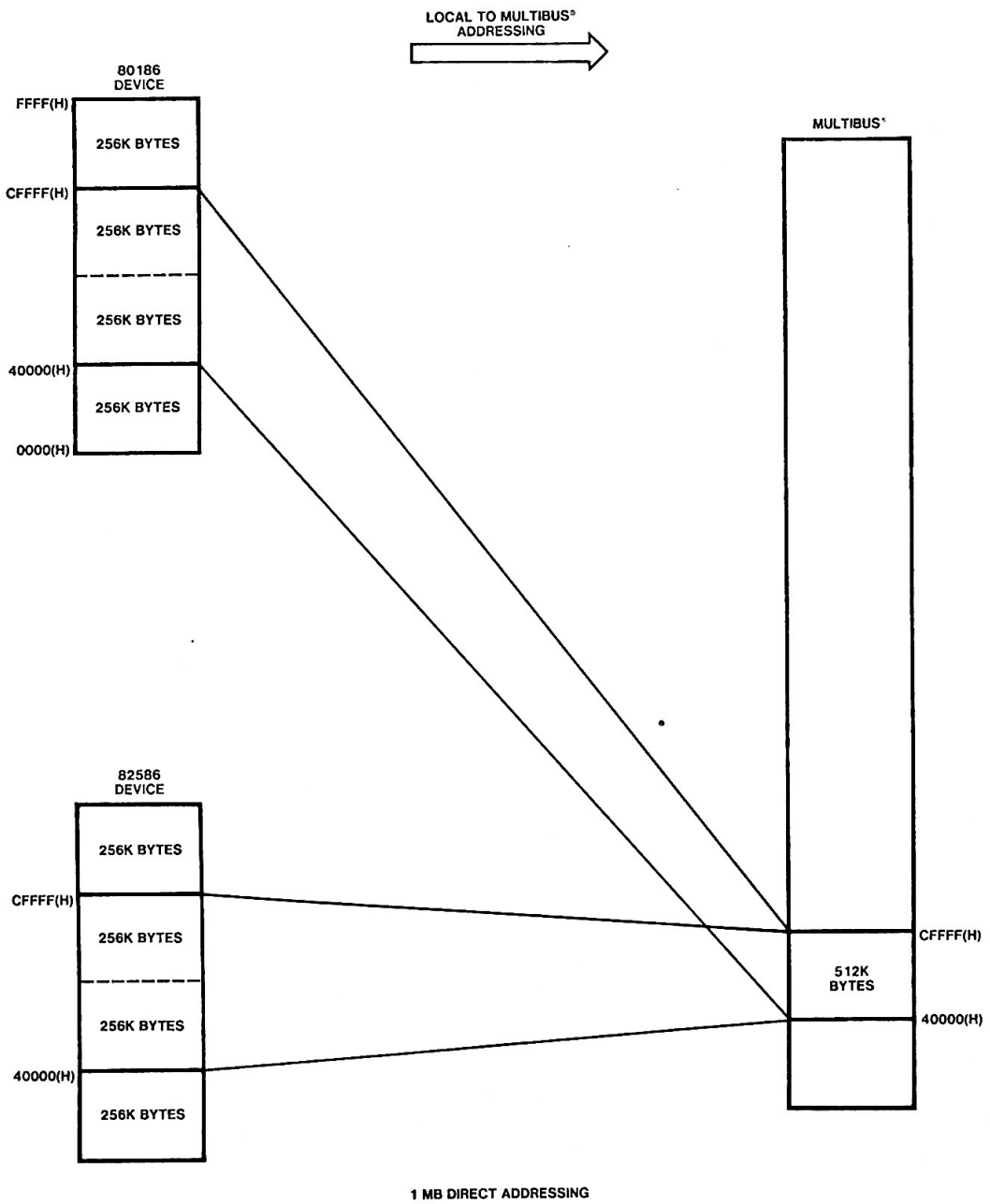


Figure 3-1. iSBC® 186/51S Board Memory Map (Sheet 2 of 4)

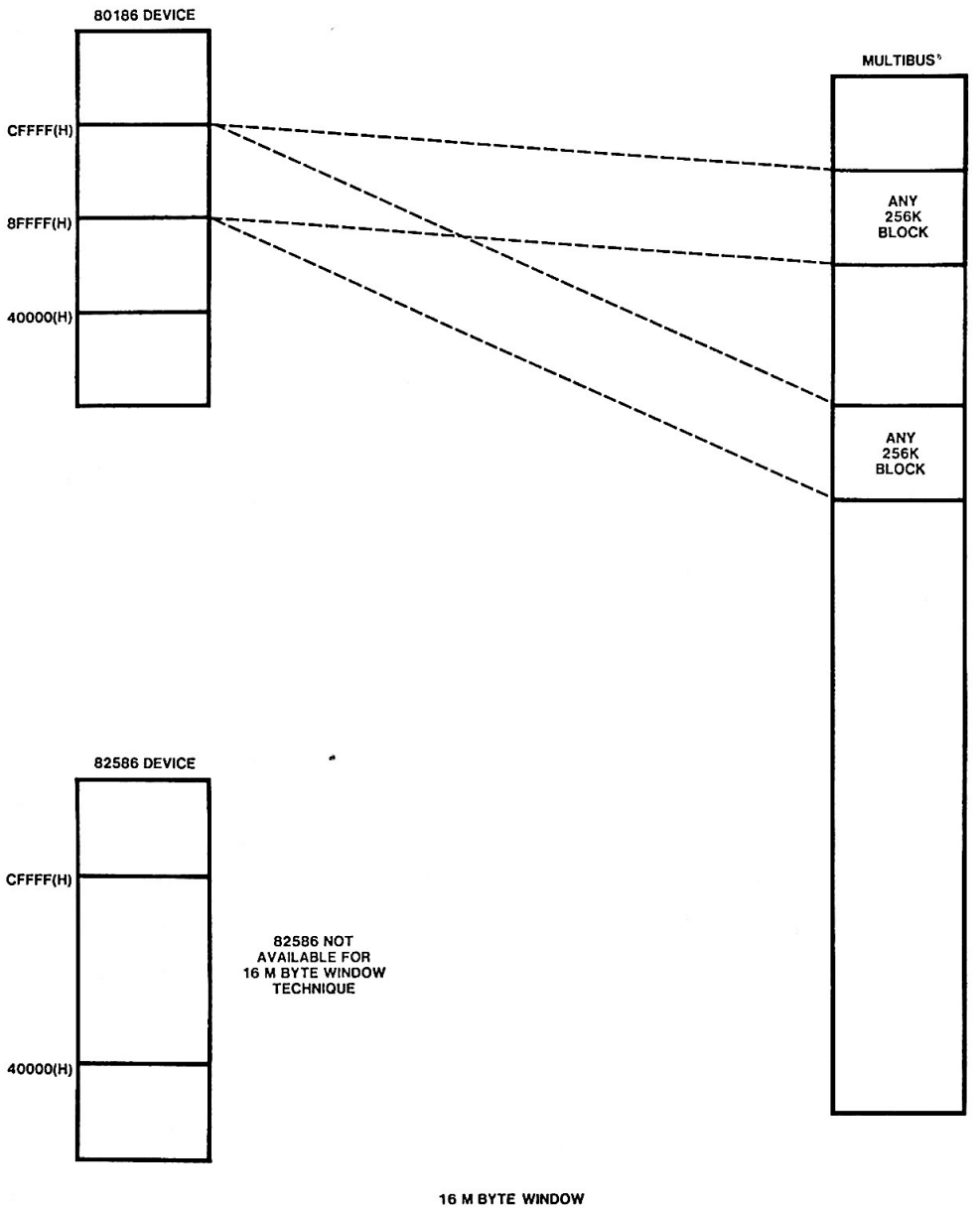


Figure 3-1. iSBC® 186/51S Board Memory Map (Sheet 3 of 4)

LOCAL MEMORY ADDRESSES

ODD ADDR (UPPER)	EVEN ADDR (LOWER)	MEMORY DEVICES			
		4K	8K	16K	32K
80186 ADDRESSES (HEX)					
U34	U51	FE000-FFFFF	FC000-FFFFF	F8000-FFFFF	F0000-FFFFF
80130A KERNAL		See Note	F8000-FBFFF	F0000-F7FFF	E0000-EFFFF
U33	U50	FA000-FBFFF	F4000-F7FFF	E8000-EFFFF	D0000-DFFFF
U32	U48	F8000-F9FFF	F0000-F3FFF	E0000-E7FFF	C0000-CFFFF
82586 ADDRESSES (HEX)					
U34	U51	FE000-FFFFF	0FC000-0FFFFF	0F8000-0FFFFF	0F0000-0FFFFF
80130A KERNAL		See Note	0F8000-0FBFFF	0F0000-0F7FFF	0E0000-0EFFFF
U33	U50	0FA000-0FBFFF	0F4000-0F7FFF	0E8000-0EFFFF	0D0000-0DFFFF
U32	U49	0F8000-0F9FFF	0F0000-0F3FFF	0E0000-0E7FFF	0C0000-0CFFFF

NOTE: IF MEMORY DEVICES OF 4K OR LESS ARE INSTALLED, THE 80130A'S iRMX KERNAL CANNOT BE USED. HOWEVER, THE TIMER AND INTERRUPT CONTROLLER OF THE 80130A CAN BE USED WITH 4K OR LESS MEMORY DEVICES.

THE 80130A MEMORY KERNAL IS 16K (TWO 8K×8 SECTIONS). WHEN 8K MEMORY DEVICES ARE USED THE TWO 8K×8 KERNAL SECTIONS FILL THE 16K OF ADDRESS SPACE. WHEN 16K DEVICES ARE USED THE 16K OF KERNAL MEMORY IS IN TWO PLACES IN THE 32K ADDRESS SPACE. WHEN 32K DEVICES ARE USED THE 16K OF KERNAL MEMORY IS SEEN IN FOUR PLACES IN THE 64K ADDRESS RANGE.

Figure 3-1. iSBC® 186/51S Board Memory Map (Sheet 4 of 4)

Table 3–1. RAM Address Range Configuration

Dual Port RAM Capacity	Local Addresses (Hex)	Type of Board Configuration
32K Bytes	18000 to 1FFFF	iSBC 186/51S Board
64K Bytes	10000 to 1FFFF	iSBC 186/51S Board
96K Bytes	08000 to 1FFFF	iSBC 186/51S Board
128K Bytes	00000 to 1FFFF	iSBC 186/51S Board
64K Bytes	30000 to 3FFFF	iSBC 186/51S board plus iSBC 304 Board
128K Bytes	20000 to 3FFFF	iSBC 186/51S board plus iSBC 304 Board
192K Bytes	10000 to 3FFFF	iSBC 186/51S board plus iSBC 304 Board
256K Bytes	00000 to 3FFFF	iSBC 186/51S board plus iSBC 304 Board

3.2.2 PROCESSOR PROGRAMMING

Some initialization of the 80186 Processor is required before the board can perform its function. The following paragraph will describe what must be done and how to do it.

3.2.3 CHIP SELECT AND READY INITIALIZATION

The chip select logic of the 80186 Processor is partially used. The UMCS (Upper Memory Chip Select) and LMCS (Lower Memory Chip Select) lines are not used at all. The VMCS needs only to be programmed for "0" wait states, external ready (ARDY) and a memory block size of 256K Bytes. The LMCS should not be programmed.

Program the Peripheral Chip Select register to zero and select two wait states using external ready to obtain access to the on-board I/O. This programming will put all on-board I/O in the 0080(H) to 00FF(H) address range. The internal (80186) peripheral register control block should not be relocated due to external I/O address decode of on-board I/O.

The iSBC 186/51S is now set-up for 1M Byte MULTIBUS master.

3.2.4 INTERNAL PERIPHERAL INTERFACE

All the iAPX 186 integrated peripherals are controlled via 16-bit registers contained within an internal 256-byte control block. This control block is mapped into I/O space in the default condition and should not be relocated. Relocating the control block will cause indeterminate results.

Internal logic in the 80186 recognizes the address and responds to the bus cycle. During bus cycles to internal registers, the bus controller will signal the operation externally.

The base address of the control block is on an even 256-byte boundary. The default address is FF00H and should not be changed. All of the defined registers within this control block can be read or written by the 80186 CPU at any time. The location of any register contained within the control block is determined by the base address of the control block.

The default address is FF00H and should not be changed.

The control block base address is programmed via a 16-bit relocation register contained within the control block of offset FEH from the base address of the control block (see Figure 3-2). It provides the upper 12 bits of the base address of the control block. In addition, bit 12 of this register determines whether the control block is mapped into I/O or memory space. In the iSBC 186/51S application bit 12 is 0 since the control block has been mapped into I/O space.

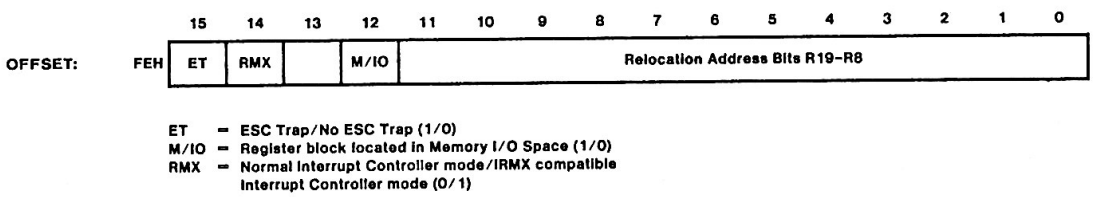


Figure 3-2. Relocation Register

The relocation register contains bits which place the interrupt controller into iRMX mode, and cause the CPU to interrupt upon encountering ESC Instructions. These are the only bits which should be programmed by the user. At RESET, the relocation register is set to 20FFH. This causes the control block to start at FF00H in I/O space. This should not be altered or unpredictable results may be obtained. An offset map of the 256-byte control register block is shown in Figure 3-3.

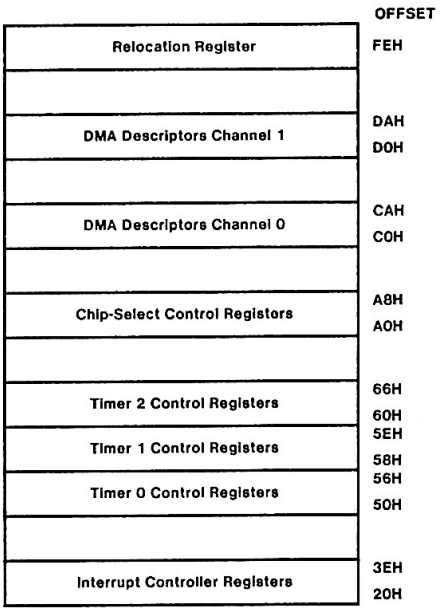


Figure 3-3. Internal Register Map

The integrated iAPX 186 peripherals operate semi-autonomously from the CPU. Access to them for the most part is via software read/write of the control and data location in the control block. Most of these registers can be both read and written. A few dedicated lines, such as interrupts and DMA request provide real-time communication between the CPU and peripherals as in a more conventional system utilizing discrete peripheral blocks. The overall interaction and function of the peripheral blocks has not substantially changed.

3.2.4.1 Chip Select Ready Generation Logic

The iAPX 186 contains logic which provides programmable chip-select generation for both memories and peripherals. In addition, it can be programmed to provide READY (or WAIT state) generation. It can also provide latches address bits A1 and A2. The chip-select lines are active for all memory and I/O cycles in their programmed areas, whether they be generated by the CPU or by the integrated DMA unit.

3.2.4.1.1 Memory Chip Selects

The iAPX 186 provides 6 memory chip select outputs for 3 address areas: upper memory, lower memory, and midrange memory. One chip select each is provided for upper memory and lower memory address areas, while four are provided for midrange memory address areas.

The range for each chip select is user-programmable and can be set to 2K, 4K, 8K, 16K, 32K, 64K, 128K (plus 1K and 256K for upper and lower chip selects). In addition, the beginning or base address of the midrange memory chip select may also be selected. Only one chip select may be programmed to be active for any memory location at a time. All chip select sizes are in bytes, whereas iAPX 186 memory is arranged in words. This means that if, for example, 16 64K x 1 memories are used, the memory block size will be 128K, not 64K.

3.2.4.1.2 Upper Memory CS

The iAPX 186 provides a chip select, called UCS/, for the top of memory. The top of memory is usually used as the system memory because after reset the iAPX 186 begins executing at memory location FFFFOH.

The upper limit of memory defined by this chip select is always FFFFH, while the lower limit is programmable. By programming the lower limit, the size of the select block is also defined. Table 3-2 shows the relationship between the base address selected and the size of the memory block obtained. In the iSBC 186/51S configuration, UCS is programmed for zero wait states, using the EXTERNAL READY; the only restriction to memory block size is it must be less than 256K Bytes.

Table 3-2. UMCS Programming Values

Starting Address (Base Address)	Memory Block Size	UMCS Value (Assuming R0=R1=R2=0)
FFC00	1K	FFF8H
FF800	2K	FFB8H
FF000	4K	FF38H
FE000	8K	FE38H
FC000	16K	FC38H
F8000	32K	F838H
F0000	64K	F038H
E0000	128K	E038H
C0000*	256K*	C038H*

* This value should not be used.

3.2.4.1.3 Lower Memory CS

In the iSBC 186/51S configuration the lower memory chip select (LCS/), should not be programmed.

3.2.4.1.4 Midrange Memory CS

The iAPX 186 provides four MCS/ lines which are active within a user-locatable memory block. This block can be located anywhere within the iAPX 186 1M Byte memory address space exclusive of the areas defined by UCS/ and LCS/. Both the base address and size of this memory block are programmable.

The size of the memory block defined by the midrange select lines, as shown in Table 3-3 is determined by bits 8-14 of the MPCS register (see Figure 3-4). This register is at location A8H in the internal control block. One and only one of bits 8-14 must be set at a time. Unpredictable operation of the MCS lines will otherwise occur. Each of the four chip-select lines is active for one of the four equal contiguous divisions of the midrange block. Thus, if the total block size is 32K, each chip select is active for 8K of memory with MCS0 being active for the first range and MCS3 being active for the last range.

To use the 16M Byte windowing capability of the iSBC 186/51S board the MMCS must be programmed with a 256K total block size and a base address of 80000(H).

The EX and MS in MPCS relate to peripheral functionality as described in Section 3.2.4.4.

Table 3-3. MMCS Programming Values

Total Block Size	Individual Select Size	MMCS Bits 14-8
8K	2K	0000001B
16K	4K	0000010B
32K	8K	0000100B
64K	16K	0001000B
128K	32K	0010000B
256K	64K	0100000B
512K	128K	1000000B

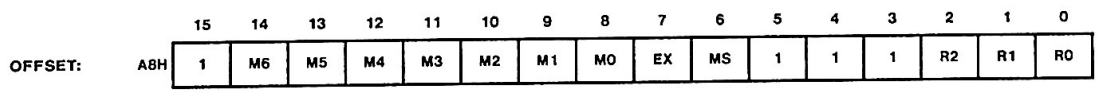


Figure 3-4. MPCS Register

The base address of the midrange memory block is defined by bits 15-9 of the MMCS register (see Figure 3-5). This register is at offset A6H in the internal control block. These bits correspond to bits A19-A13 of the 20-bit memory address. Bits A12-A0 of the base address are always 0. The base address may be set at any integer multiple of the size of the total memory block selected. For example, if the midrange block size is 32K (or the size of the block for which each MCS/ line is active is 8K), the block could be located at 10000H or 18000H, but not at 14000H, since the first few integer multiples of a 32K memory block are 0H, 8000H, 10000, 180000H, etc. After reset, the contents of both of these registers is undefined. However, none of the MCS/ lines will be active until both the MMCS and MPCS registers are accessed.

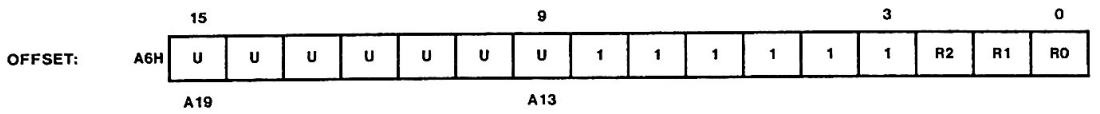


Figure 3-5. MMCS Register

MMCS bits R2-R0 specify READY mode of operation for all midrange chip selects. All devices in midrange memory must use the same number of WAIT states.

For a 16M Byte window, the base address is programmed at 80000(H) and zero wait states, using external ready: Example 81F8H.

3.2.4.2 Ready Generation Logic

The iAXP 186 can generate a "READY" signal internally for each of the memory or peripheral CS/ lines. The number of WAIT states to be inserted for each peripheral or memory is programmable to provide 0-3 wait states for all accesses to the area for which the chip select is active. In addition, the iAPX 186 may be programmed to either ignore external READY for each chip-select range individually or to factor external READY with the integrated ready generator.

READY control consists of 3 bits for each CS/ line or group of lines generated by the 80186. The interpretation of the ready bits is shown in Table 3-4.

The internal ready generator operates in parallel with external READY, not in series if the external READY is used (R2 = 0). This means, for example, if the internal generator is set to insert two wait states, but activity on the external READY lines inserts four wait states, the processor will insert four wait states, not six. This is because the two wait states generated by internal generator overlapped

the first two wait states generated by the external ready signal. Note that the external ARDY and SRDY lines are always ignored during cycles accessing internal peripherals.

R2-R0 of each control word specifies the READY mode for the corresponding block, with the exception of the peripheral chip selects: R2-R0 of PACS set the PCS0-3 READY mode, R2-R0 of MPCS set the PCS4-6 READY mode.

Table 3-4. READY Bits Programming

R2	R1	R0	Number of WAIT States Generated
0	0	0	0 wait states, external, RDY also used.
0	0	0	1 wait state inserted, external RDY also used.
0	1	0	2 wait states inserted, external RDY also used.
0	1	1	3 wait states inserted, external RDY also used.
1	0	0	0 wait states, external RDY ignored.
1	0	1	1 wait state inserted, external RDY ignored.
1	1	0	2 wait states inserted, external RDY ignored.
1	1	1	3 wait states inserted, external RDY ignored.

3.2.4.2.1 Chip Select/Ready Logic and Reset

Upon reset, the Chip-Select/Ready Logic will perform the following actions:

- All chip-select outputs will be driven HIGH.
- Upon leaving RESET, the UCS line will be programmed to provide chip selects to a 1K block with the accompanying READY control bits set at 011 to allow the maximum number of internal wait states in conjunction with external READY consideration (i.e., UMCS resets to FFFBH).
- No other chip select or READY control registers have any predefined values after RESET. They will not become active until the CPU accesses their control registers. Both the PACS and MPCS registers must be accessed before the PCS lines will become active.

3.2.4.3 Peripheral Chip Selects

The 80186 can generate chip selects for up to seven peripheral devices. These chip selects are active for seven contiguous blocks of 128K Bytes above a programmable base address. This base address may be located in either memory or I/O space.

Seven CS lines called PCSO/ through PCS6/ are generated by the iAPX 186. The base address is user programmable; however it can only be a multiple of 1K Bytes, i.e., the least significant 10 bits of the starting address are always 0.

PCS5/ and PCS6/ can also be programmed to provide latched address bits A1,A2. If so programmed, they cannot be used as peripheral selects. These outputs can be connected directly to the A0, A1 pins used for selecting internal registers of 8-bit peripheral chips. This scheme simplifies the hardware interface because the 8-bit registers of peripherals are simply treated as 16-bit registers located on even boundaries in I/O space or memory space where only the lower 8-bits of the register are significant: the upper 8-bits are "don't cares."

The starting address of the peripheral chip-select block is defined by the PACS register (see Figure 3-6). This register is located at offset A4H in the internal control block. Bits 15-6 of this register correspond to bits 19-10 of the 20-bit Programmable Base Address (PBA) of the peripheral chip-select block. Bits 9-0 of the PBA of the peripheral chip-select block are all zeros. If the chip-select block is located in I/O space, bits 12-15 must be programmed zero, since the I/O address is only 16 bits wide. Table 3-5 shows the address range of each peripheral chip select with respect to the PBA contained in PACS register.

The base address must be programmed to zero and two wait states selected, using external ready to ensure proper operation of the iSBC 186/51S board.

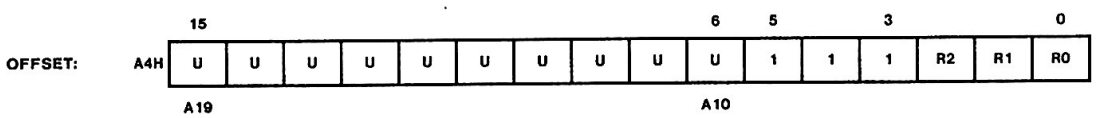


Figure 3-6. PACS Register

Table 3-5. PCS Address Ranges

PCS Line	Active Between Locations
PCSO	PBA - PBA + 127
PCS1	PBA + 128 - PBA + 255
PCS2	PBA + 256 - PBA + 383
PCS3	PBA + 384 - PBA + 511
PCS4	PBA + 512 - PBA + 639
PCS5	PBA + 640 - PBA + 767
PCS6	PBA + 768 - PBA + 895

The user should program bits 15-6 to correspond to the desired peripheral base location. PACS bits 0-2 are used to specify READY mode for PCS0/-PCS3/. Peripheral chip select must be mapped into I/O space.

The mode of operation of the peripheral chip selects is defined by the MPCS register (which is also used to set the size of the midrange memory chip-select block, see Figure 3-7). This register located at offset A8H in the internal control block. Bit 7 is used to select the function of PCS5/ and PCS6/, while bit 6 is used to select whether the peripheral chip selects are mapped into memory or I/O space. Table 3-6 describes the programming of these bits. After reset, the contents of both the MPCS and the PACS registers are undefined, however, none of the PCS lines will be active until both of the MPCS and PACS registers are accessed.

MPCS bits 0-2 are used to specify READY mode for PCS4 - PCS6 as outlined below.

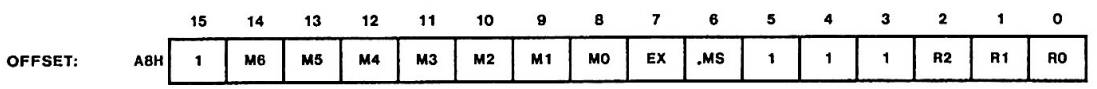


Figure 3-7. MPCS Register

Table 3-6. MS, EX Programming Values

Bit	Description
MS	1 = Peripherals mapped into memory space 0 = Peripherals mapped into I/O space (1)
EX	0 = 5 PCS/ lines. A1, A2 provided 1 = 7 PCS/ lines. A1, A2 are not provided

NOTE: In the iSBC 186/51S application, MS must be 0 and EX must be 1.

3.2.5 16M BYTE MASTER INITIALIZATION

The iSBC-186/51S board can be operated as either a 1M Byte MULTIBUS Master as described in Section 3.2.3 or as a 16 M-byte MULTIBUS Master. To obtain the 16M Byte capability, the midrange chip selects (MCS0-MCS3) of the 80186 as well as the 8283 16M Byte address latch (U86) must be programmed. When operating as a 16M Byte master the iSBC 186/51S board sees the MULTIBUS interface address space as 64 256K Byte segments, which do not overlap. Six latched lines D2 through D7 are to be accessed. Thus, the six latched address lines are appended to the 18 lower MULTIBUS address lines creating the 24 address lines required.

To latch the upper six address bits an I/O write to latch U84 is performed (address 00DO). The most significant address bit to the latch is the most significant data location.

To enable the 16M Byte mode, the midrange chip select (MCS0 through MCS3) of the 80186 must be initialized, see Section 3.2.4.1.4 for the initialization programming. The 16M Byte window can be positioned in any of the 256K Byte segments of the MULTIBUS address space. If the segment between 080000H and 0BFFFFH is selected, the total block size should be set to 256K Bytes with a base of 080000H. The ready should be selected for zero wait states using external ready (see Section 3.2.4.3).

With the programming described above accesses by the 80186 to locations 80000H-B0000H within the 1M Byte address space will be MULTIBUS addresses with the six latched address bits being the upper MULTIBUS addresses.

3.2.6 80186 PERIPHERAL INITIALIZATION

There is no special initialization programming required for the DMA channels or timers of the 80186 processor. When used they should be programmed as in Sections 3.2.7 and 3.2.8.

The 80186 interrupt controller must be in the iRMX 86 compatability mode. In this mode the external 80130A programmable interrupt controller is the master interrupt controller. The interrupt controller on the 80186 processor is slaved to it. For operation in this mode the interrupt controller on the 80186 should be initialized as specified in Section 3.2.9. Section 3.2.10 describes 80130A programming.

3.2.7 80186 DMA PROGRAMMING

The following paragraphs describe DMA programming of the 80186.

3.2.7.1 DMA Channels

The 80186 DMA controller provides two independent high-speed DMA channels. Data transfers can occur between memory and I/O spaces (e.g., Memory to I/O) or within the same space (e.g., Memory to Memory or I/O to I/O). Data can be transferred either in bytes (8 bits) or in words (16 bits) to or from even or odd addresses. Each DMA channel maintains both a 20-bit source and destination pointer which can be optionally incremented or decremented after each data transfer (by one or two depending on byte or word transfers). Each data transfer consumes 2 bus cycles (a minimum of 8 clocks), one cycle to fetch data and the other to store data. This provides a maximum data transfer rate of one M-word/sec or 2M Bytes/sec.

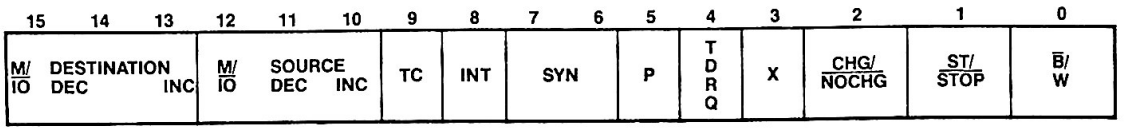
3.2.7.1.1 DMA Operation

Each channel has six registers in the control block which define each channel's specific operation. The control registers consists of a 20-bit Source pointer (2 words), a 20-bit Destination pointer(2 words), a 16-bit Transfer Counter, and a 16-bit Control Word. The format of the DMA Control Blocks is shown in Table 3-7. The Transfer Count Register (TC) specifies the number of DMA transfers to be

performed. Up to 64K byte or word transfers can be performed with automatic termination. The Control Word defines the channel's operation (see Figure 3-8). All registers may be modified or altered during any DMA activity. Any changes made to these registers will be reflected immediately in DMA operation.

Table 3-7. DMA Control Block Format

Register Name	Register Address	
	Ch.0	Ch.1
Control Word	FFCAH	FFDAH
Transfer Count	FFC8H	FFD8H
Destination Pointer (upper 4 bits)	FFC6H	FFD6H
Destination Pointer	FFC4H	FFD4H
Source Pointer (upper 4 bits)	FFC2H	FFD2H
Source Pointer	FFC0H	FFD0H



X = DON'T CARE.

Figure 3-8. DMA Control Register

3.2.7.1.2 DMA Channel Control Word Register

Each DMA Channel Control Word determines the mode of operation for the particular 80186 DMA channel. This register specifies:

- o the mode of synchronization;
- o whether bytes or words will be transferred;
- o whether interrupts will be generated after the last transfer;
- o whether DMA activity will cease after the last transfer;
- o the relative priority of the DMA channel with respect to the other DMA channel;
- o whether the source pointer will be incremented, decremented, or maintained constant after each transfer;
- o whether the source pointer addresses memory or I/O space;

- o whether the destination pointer will be incremented, decremented, or maintained constant after each transfer; and
- o whether the destination pointer will address memory or I/O space.

The DMA channel control registers may be changed while the channel is in operation. However, any changes made during operation will affect the current DMA transfer.

3.2.7.1.3 DMA Control Word Bit Descriptions

B/W: Byte/Word (0/1) Transfers.

ST/STOP/: Start/stop (1/0) Channel.

CHG/NOCHG/: Change/Do not change (1/0) ST/STOP/ bit. If this bit is set when writing to the control word, the ST/STOP/ bit will be programmed by the write to the control word. If this bit is cleared when writing the control word, the ST/STOP/ bit will not be altered. This bit is not stored; it will always be a 0 on read.

INT: Enable interrupts to CPU on byte count termination.

TC: If set, DMA will terminate when the contents of the Transfer Count register reach zero. The ST/STOP/ bit will also be reset at this point if TC is set. If this bit is cleared, the DMA unit will decrement the transfer count register for each DMA cycle, but the DMA transfer will not stop when the contents of the TC register reach zero.

SYN: (2 bits)

00 No Synchronization.

NOTE: The ST bit will be cleared automatically when the contents of the TC register reach zero regardless of the state of the TC bit.

01 Source synchronization.

10 Destination Synchronization.

11 Unused.

SOURCE: INC Increment source pointer by 1 or 2 (depends on B/W) after each transfer.

M/IO/ Source pointer is in M/IO space (1/0).

DEC Decrement source pointer by 1 or 2 (depends on B/W) after each transfer.

DEST: INC Increment destination pointer by 1 or 2 (B/W) after each transfer

M/IO/ Destination pointer is in M/IO space (1/0).

DEC Decrement destination pointer by 1 or 2 (depending on B/W) after each transfer.

P: Channel priority-relative to other channel.
0 low priority.
1 high priority.
Channels will alternate cycles if both set at same priority level.

TDRQ 0: Disable DMA requests from timer 2.

1: Enable DMA requests from timer 2.

Bit 3 Bit 3 is not used.

If both INC and DEC are specified for the same pointer, the pointer will remain constant after each cycle.

3.2.7.1.4 DMA Destination and Source Pointer Registers

Each DMA channel maintains a 20-bit source and a 20-bit destination pointer. Each of these pointers takes up two full 16-bit registers in the peripheral control block. The lower four bits of the upper register contain the upper four bits of the 20-bit physical address (see Figure 3-9). These pointers may be individually incremented or decremented after each transfer. If word transfers are performed the pointer is incremented or decremented by two. Each pointer may point into either memory or I/O space. Since the DMA channels can perform transfers to or from odd addresses, there is no restriction on values for the pointer registers. Higher transfer rates can be obtained if all word transfers are performed to even addresses, since this will allow data to be accessed in a single memory access.

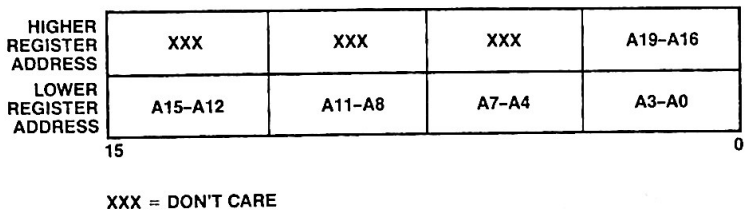


Figure 3-9. DMA Memory Pointer Register Format

3.2.7.1.5 DMA Transfer Count Register

Each DMA channel maintains a 16-bit transfer count register (TC). This register is decremented after every DMA cycle, regardless of the state of the TC bit in the DMA Control Register. If the TC bit in the DMA control word is set, however, DMA activity will terminate when the transfer count register reaches zero.

3.2.7.1.6 DMA Requests

Data transfers may be either source or destination synchronized, that is either the source of the data or the destination of the data may request the data transfer. In addition, DMA transfers may be unsynchronized; that is the transfer will take place continually until the correct number of transfers has occurred. When source or unsynchronized transfers are performed, the DMA channel may begin another transfer immediately after the end of a previous DMA transfer. This allows a complete transfer to take place every 2 bus cycles or eight clock cycles (assuming not wait states). No prefetching occurs when destination synchronization is performed, however. Data will not be fetched from the source address until the destination device signals that it is ready to receive it. When destination synchronized transfers are requested, the DMA controller will relinquish control of the bus after every transfer. If no other bus activity is initiated, another DMA cycle will begin after two processor clocks. This is done to allow the destination device time to remove its request if another transfer is not desired. Since the DMA controller will relinquish the bus, the CPU can initiate a bus cycle. As a result, a complete bus cycle will often be inserted between destination synchronized transfers. These lead to the maximum DMA transfer rates shown in Table 3-8.

Table 3-8. Maximum DMA Transfer Rates

Type of Synchronization Selected	CPU Running	CPU Halted
Unsynchronized	2M Bytes/sec	2M Bytes/sec
Source Synch	2M Bytes/sec	2M Bytes/sec
Destination Synch	1.3M Bytes/sec	1.5M Bytes/sec

3.2.7.1.7 DMA Acknowledge

No explicit DMA acknowledge pulse is provided. Since both source and destination pointers are maintained, a read from a requesting source, or a write to a requesting destination should be used as the DMA acknoweldge signal. Since the chip-select lines can be programmed to be active for a given block of memory or I/O space, and the DMA pointers can be programmed to point to the same given block, a chip-select line could be used to indicate a DMA acknowledge.

3.2.7.1.8 DMA Priority

The DMA channels may be programmed such that one channel is alway given priority over the other, or they may be programmed such as to alternate cycles when both have DMA requests pending. DMA cycles always have priority over internal CPU cycles except between locked memory accesses or word accesses the odd memory locations; however, an external bus hold takes priority over an internal DMA cycle. Because an interrupt request cannot suspend a DMA operation and the CPU cannot access memory during a DMA cycle, interrupt latency time will suffer during sequences of continuous DMA cycles. An NMI request, however, will cause all internal DMA activity to halt. This allows the CPU to quickly respond to the NMI request.

3.2.7.1.9 DMA Programming

DMA cycles will occur whenever the ST/STOP bit of the Control Register is set. If synchronized transfers are programmed, a DRQ must also have been generated.

Therefore, the source and destination transfer pointers, and the transfer count register (if used) must be programmed before this bit is set.

Each DMA register may be modified while the channel is in operation. If the CHG/NOCHG bit is cleared when the control register is written, the ST/STOP bit of the control register will not be modified by the write. If multiple channel registers are modified, it is recommended that a LOCKET string transfer be used to prevent a DMA transfer from occurring between updates to the channel registers.

3.2.7.1.10 DMA Channels and Reset

Upon RESET, the DMA channels will perform the following actions:

- o The Start/Stop bit for each channel will be reset to STOP.
- o Any transfer in progress is aborted.

3.2.8 80186 TIMER PROGRAMMING

The following paragraphs describe the 80186 timers and their programming.

3.2.8.1 Timers

The 80186 provides three internal 16-bit programmable timers. Two of these are highly flexible and are connected to four external pins (2 per timer). They can be used to count external events, time external events, generate nonrepetitive waveforms, etc. The third timer is not connected to any external pins, and is useful for real-time coding and time delay applications. In addition, this third timer can be used as a prescaler to the other two, or as a DMA request source.

3.2.8.1.1 Timers Operation

The timers are controlled by 11 16-bit registers in the internal peripheral control block. The configuration of these registers is shown in Table 3-9. The count register contains the current value of the timer. It can be read or written at any time independent of whether the timer is running or not. The value of this register will be incremented for each timer event. Each of the timers is equipped with MAX

COUNT register, which defines the maximum count the timer will reach. After reaching the MAX count register value, the timer count value will reset to zero during that same clock, i.e., the maximum count value is never stored in the count register, which enables the timers to alternate their count between two different MAX COUNT value programmed by the user. If a single MAX COUNT register, which enables the timers to alternate their count between two different MAX COUNT values programmed by the user. If a single MAX COUNT register is used, the timer output pin will switch LOW for a single clock, two clocks after the maximum count value has been reached. In the dual MAX COUNT register mode , the output pin will indicate which MAX COUNT register is currently in use, thus allowing nearly complete freedom in selecting waveform duty cycles. For the timers with two MAX count registers, the RIU bit in the control register determines which timer is used for the comparison.

Table 3-9. Timer Control Block Format

Register Name	Register Offset		
	Tmr.0	Tmr.1	Tmr.2
Mode/Control Word	FF56H	FF5EH	FF66H
Max Count B	FF54H	FF5CH	Not Present
Max Count A	FF52H	FF5AH	FF62H
Count Register	FF50H	FF58H	FF60H

Each timer gets serviced every fourth CPU-clock cycle, and thus can operate at speeds up to one-quarter the internal clock frequency (one-eighth the crystal rate). External clocking of the timers may be done at up to a rate of one-quarter of the internal CPU-clock rate (1.5 MHz for an 6 MHz CPU clock). Due to internal synchronization and pipelining of the timer circuitry, a timer output may take up to 6 clocks to respond to any individual clock or gate input.

Since the count registers and the maximum count registers are all 16 bits wide, 16 bits of resolution are provided. Any Read or Write access to the timers will add one wait state to the minimum four-clock bus cycle, however. This is needed to synchronize and coorrdinate the internal data flows between the internal timers and the internal bus.

The timers have several programmable options.

- o All three timers can be set to halt or continue on a terminal count.
- o Timers 0 and 1 can select between internal and external clocks, alternate between MAX count registers and be set to retrigger on external events.
- o The timers may be programmed to cause an interrupt on terminal count.

These options are selectable via the timer mode/ control word.

3.2.8.1.2 Timer Modes/Control Register

The mode/control register (see Figure 3-10) allows the user to program the specific mode of operation or check the current programmed status for any of the three integrated timers.

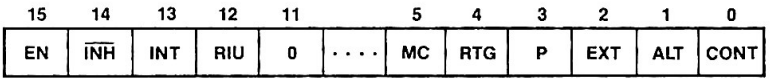


Figure 3-10. Timer Mode/Control Register

ALT: The ALT bit determines which of two MAX COUNT registers is used for count comparison. If ALT = 0, register A for that timer is always used, while if ALT = 1, the comparison will alternate between register A and register B when each maximum count is reached. This alternation allows the user to change one MAX COUNT register while the other is being used, and thus provides a method of generating non-repetitive waveforms. Square waves and pulse outputs of any duty cycles are a subset of available signals obtained by not changing the final count registers. The ALT bit also determines the function of the timer output pin. If ALT is zero, the output pin will reflect the current MAX COUNT register being used (0/1 for B/A).

CONT: Setting the CONT bit causes the associated timer to run continously, while resetting it causes the timer to halt upon maximum count. If CONT = 0 and ALT = 1, the timer will count to the MAX COUNT register A value, reset, count to the register B value, reset and halt.

EXT: The external bit selects between internal and external clocking for the timer. The external signal may asynchronous with respect to the 80186 clock. If this bit is set, the timer will count LOW-to-HIGH transitions on the input pin. If cleared, it will count an internal clock while using the input pin for control. In this mode, the function of the external pin is defined by the RTG bit. The maximum input to output transition latency time may be as much as 6 clocks. However, clock inputs may be pipelined as close together as every 4 clocks without losing clock pulses.

P: The prescaler bit is ignored unless internal clocking has been selected (EXT = 0). If the P bit is a zero, the timer will count at one-fourth the internal CPU clock rate. If the P bit is a one, the output of the timer 2 will be used as a clock for the timer. Note that the user must initialize and start timer 2 to obtain the prescaled clock.

RTG: The retrigger bit is only active for internal clocking (EXT = 0). In this case it determines the control function provided by the input pin.

If RTG = 0, the input level gates the internal clock on and off. If the input pin is HIGH, the timer will count; if the input pin is LOW, the timer will hold its value. As indicated previously, the input signal may be asynchronous with respect to the 80186 clock.

When RTG = 1, the input pin detects LOW-to-HIGH transitions. The first such transition starts the timer running, clearing the timer value to zero on the first clock, and then incrementing thereafter. Further transitions on the input pin will again reset the timer to zero, from which it will start counting up again. If CONT =0 , when the timer has reached maximum count, the EN bit will be cleared, inhibiting further timer activity.

EN: The enable bit provides programmer control over the timer's RUN/HALT status. When set, the timer is enabled to increment subject to the input pin constraints in

the internal clock mode (discussed previously). When cleared, the timer will be inhibited from counting. All input pin transitions during the time EN is zero will be ignored. If CONT is zero, the EN bit is automatically cleared upon maximum count.

INH: The inhibit bit allows for selective updating of the enable (EN) bit. If INH is a one during the write to the mode/control word, then the state of the EN bit will be modified by the write. If INH is a zero during the write, the EN bit will be unaffected by the operation. This bit is not stored; it will always be a 0 on a read.

INT: The INT bit, when set, enables interrupts from the timer, which will be generated on every terminal count. If the timer is configured in dual MAX COUNT register mode, an interrupt will be generated each time the value in MAX COUNT register A is reached, and each time the value in MAX COUNT register B is reached. If this enable bit is cleared after the interrupt request has been generated, but before a pending interrupt is serviced, the interrupt request will still be in force. (The request is latched in the Interrupt Controller).

MC: The Maximum Count bit is set whenever the timer reaches its final maximum count value. If the timer is configured in dual MAX COUNT register mode, this bit will be set each time the value in MAX COUNT register A is reached, and each time the value in MAX COUNT register B is reached. If this enable bit is cleared after the interrupt request has been generated, but before a pending interrupt is serviced, the interrupt request will still be in force. (The request is latched in the Interrupt Controller).

RIU: The Register In Use bit indicates which MAX COUNT register is currently being used for comparison to the timer count value. A zero value indicates register A. The RIU bit cannot be written, i.e., its value is not affected when the control register is written. It is always cleared when the ALT bit is zero.

Not all mode bits are provided for timer 2. Certain bits are hardwired as indicated below:

ALT = 0, EXT = 0, P = 0, RTG = 0, RIU = 0

3.2.8.1.3 Count Registers

Each of the three timers has a 16-bit count register. The current contents of this register may be read or written by the processor at any time. If the register is written into while the timer is counting, the new value will take effect in the current count cycle.

3.2.8.1.4 Max Count Registers

Timers 0 and 1 have two MAX COUNT registers, while timer 2 has a single MAX COUNT register. These contain the number of events the timer will count. In timers 0 and 1, the MAX COUNT register used can alternate between the two max count values whenever the current maximum count is reached. The condition which causes a timer to reset is equivalent between the current count value and the max count being used. This means that if the count is changed to be above the max count value, or if the max count value is changed to be below the current value, the timer will not reset to zero, but rather will count to its maximum value, "wrap around" to zero, then count until the max count is reached.

3.2.9 80186 iRMX™86 MODE TIMING PROGRAMMING

The following paragraphs describe iRMX 86 mode programming.

3.2.9.1 iRMX™86 Compatibility Mode

This mode allows iRMX 86-80186 compatibility. The interrupt model of iRMX 86 requires one master interrupt controller and multiple slaves. When iRMX mode is used, the internal 80186 interrupt controller will be used as a slave controller to an external master interrupt controller, the Intel 80130A. The internal 80186 resources will be monitored through the internal interrupt controller, while the external 80130A controller functions as the system master interrupt controller.

Upon reset, the 80186 interrupt controller will be in the non-iRMX 86 mode of operation. To set the controller in the iRMX mode, bit 14 of the Relocation Register should be set, see Figure 3-11.

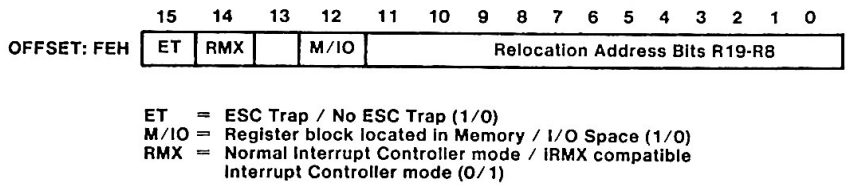


Figure 3-11. Relocation Register (iRMX™86 Capatibility Mode)

The iRMX 86 operating system requires peripherals to be assigned fixed priority levels. This is incompatible with the normal operation of the 80186 interrupt controller. Therefore, the initialization software must program the proper priority levels for each source. The required priority levels for the internal interrupt sources in iRMX mode are shown in Table 3-10.

The level of assignments must remain fixed in the iRMX 86 mode of operation.

Table 3-10. Internal Source Priority Level

Priority Level	Interrupt Source
0	Timer 0
1	(reserved)
2	DMA 0
3	DMA1
4	Timer 1
5	Timer 2

3.2.9.2 iRMX™86 Mode External Interface

The configuration of the 80186 with respect to an external 80130A master is shown in Figure 3-12. The INTO input 80186 (pin 45) is used as the 80186 CPU interrupt input. INT3 80186 (pin 41) functions as an output to send the 80186 slave-interrupt request to one of the eight master PIC inputs (IR4). INT1/ (pin 44) through a PAL is used as a slave-select input.

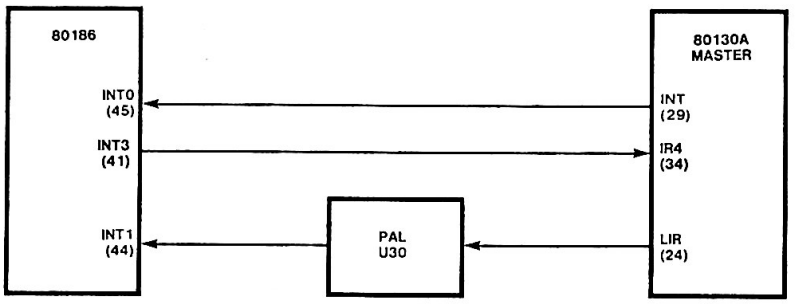


Figure 3-12. iRMX™ 86 Interrupt Controller Interconnection

3.2.9.3 Interrupt Nesting

iRMX 86 mode operation allows nesting of interrupt requests. When an interrupt is acknowledged, the priority logic masks off all priority levels except those with equal or higher priority.

3.2.9.4 Vector Generation in the iRMX™ 86 Mode

Vector generation in iRMX mode is exactly like that of an 8259A slave. The interrupt controller generates an 8-bit vector which the CPU multiplies by four and uses an address into a vector table. The significant five bits of the vector are user-programmable while the lower three bits are generated by the priority logic. These bits represent the encoding of the priority level requesting service. The significant five bits of the vector are programmed by writing to the Interrupt Vector register at FF20H (includes 20H offset).

3.2.9.5 Specific End of Interrupt

In iRMX mode the specific EOI command operates to reset an in-service bit of specific priority. The user supplies a 3-bit priority-level value that points to an in-service bit to be reset. The command is executed by writing the correct value in the Specific EOI register at FF22H (includes 20H offset).

3.2.9.6 Interrupt Controller Registers in the iRMX™ 86 Mode

All control and command registers are located inside the internal peripheral control block. Figure 3-13 shows the offsets of these registers.

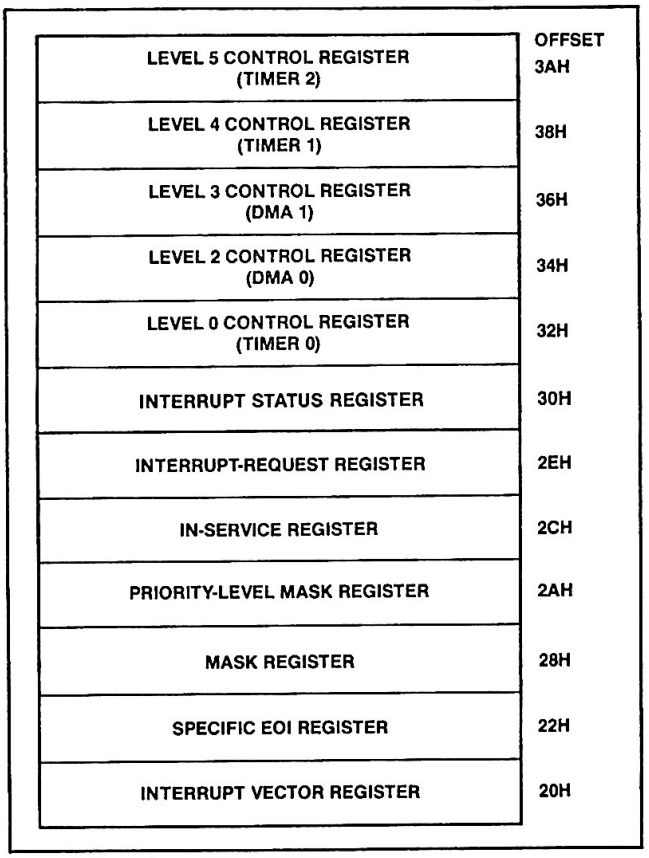


Figure 3-13. Interrupt Controller Registers (iRMX™ 86 Mode)

3.2.9.7 End of Interrupt Register

The end of interrupt register is a command register which can only be written. The format of this register is shown in Figure 3-14. It initiates an EOI Command when written by the 80186 CPU.

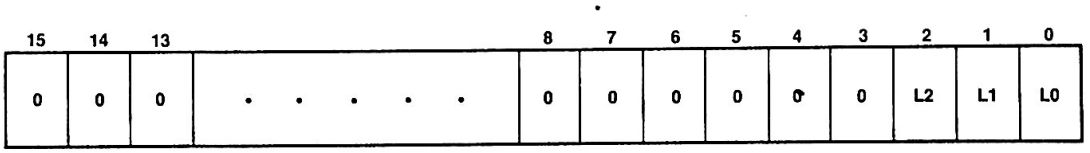


Figure 3-14. Specific EOI Register Format

The bits in the EOI Register are encoded as follows:

L_X: Encoded value indicating the priority of the IS bit to be reset.

3.2.9.8 In-Service Register

This register can be read from or written into. It contains the in-service bit for each of the internal interrupt sources. The format for this register is shown in Figure 3-15. Bit positions 2 and 3 correspond to the DMA channels; positions, 0, 4, and 5 correspond to the integral timers. The source IS bit is set when the processor acknowledges its interrupt request.

3.2.9.9 Interrupt Request Register

This register indicates which internal peripherals have interrupt requests pending. The format of this register is shown in Figure 3-15. The interrupt request bits are set when a request arrives fron an internal source, and are reset when the processor acknowledges the request.

3.2.9.10 Mask Register

This register contains a mask bit for each interrupt source. The format for this register is shown in Figure 3-15. If the bit in this register corresponding to a particular interrupt source is set, any interrupts from that source will be masked. These mask bits are exactly the same bits which are used in the individual control register, i.e., changing the state of a mask bit in this register will also change the state of the mask bit in the individual interrupt control register corresponding to the bit.

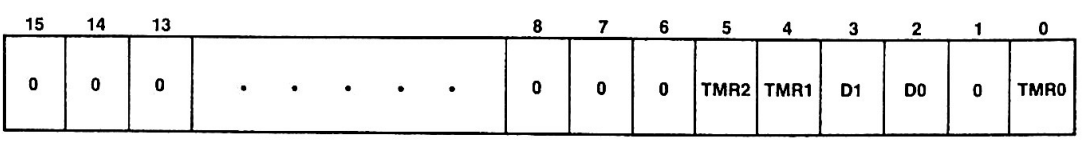


Figure 3-15. In-Service Interrupt Request and Mask Register Format

3.2.9.11 Control Registers

These registers are the control words for all the internal interrupt sources. The format of these registers is shown in Figure 3-16. Each of the timers and both of the DMA channels have their own Control Register.

The bits of the Control Registers are as follows:

pr_x: 3-bit encoded field indicating a priority level for the source; note that each source must be programmed at specified levels.

msk: mask bit for the priority level indicated by pr_x bits.

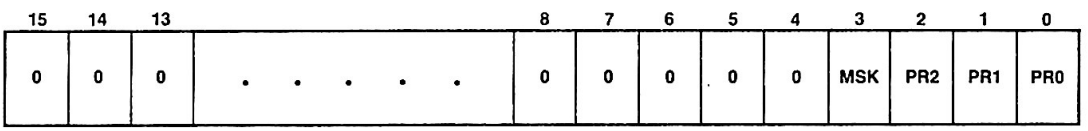


Figure 3-16. Control Word Format

3.2.9.12 Interrupt Vector Register

This register provides the upper five bits of the interrupt vector address. The format of this register is shown in Figure 3-17. The interrupt controller itself provides the lower three bits of the interrupt vector as determined by the priority level of the interrupt request.

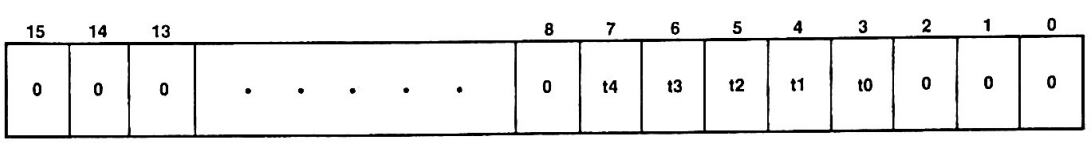


Figure 3-17. Interrupt Vector Register Format

The format of the bits in this register is:

t_x: 5-bit field indicating the upper five bits of the vector address.

3.2.9.13 Priority Level Mask Register

This register, Figure 3-18, indicates the lowest priority level interrupt which will be serviced.

The encoding of the bits in this register is:

m_x: 3 bit encoded field indication priority-level value. All levels of lower prioirty will be masked.

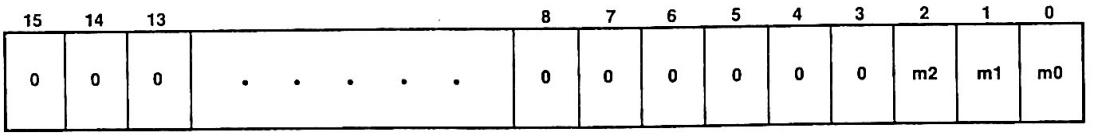


Figure 3-18. Priority Level Mask Register

3.2.9.14 Interrupt Controller and Reset

Upon RESET, the interrupt controller will perform the following actions:

- All SFNM bits reset to 0, implying Fully Nested Mode.
- All PR bits in the various control registers set to 1. This places all sources at lowest priority (level 111).
- All LTM bits reset to 0, resulting in edge-sense mode.
- All Interrupt Service bits reset to 0.
- All Interrupt Requests bits reset to 0.
- All MSK (Interrupt Mask) bits set to 1 (mask).
- All C (Cascade) bits reset to 0 (non-cascade).
- All PRM (Priority Mask) bits set to 1, implying no levels masked.
- Initialized to non-iRMX 86 mode.

3.2.10 80130A PIC PROGRAMMING

The following paragraphs describe 80130A PIC programming.

3.2.10.1 Read Only Memory (ROM)

The 80130A contains 128K Bits of ROM. The ROM is accessed on the data bus by activating of the MEMCS pin (KERNEL CS/signal) and a memory read or instruction fetch cycle. The BHE/ input (S7/BHE) signal controls whether the ROM is addressed as 8K of 16-bit words of program data or 16K of 8-bit bytes of program data. The ROM is compatible with the 80186 processor.

3.2.10.2 Programmable Interrupt Controller (PIC)

The PIC control registers are accessed as byte values on even address boundaries. Read and write operation are controlled internally by I/O read or I/O write signal generated by the BIU.

Programming of the PIC is done by accessing the control words in the I/O space located at addresses E0H and E2H, while IOCS (80130A I/O CS/ signal) is held low. The register address locations are:

Register	Address
Interrupt Request Register	E0H
In-Service Register	E0H
Interrupt Mask Register	E2H
Initialization Control Word 1	E0H
Initialization Control Word 2	E2H
Initialization Control Word 3	E2H
Initialization Control Word 4	E2H
Initialization Control Word 5	E2H
Initialization Control Word 6	E2H
Operation Control Word 1	E1H
Operation Control Word 2	E0H
Operation Control Word 3	E0H

The interrupts at the IR0 through IR7 input lines are handled by two registers, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR stores all interrupt levels being serviced. A logic block determines the priorities of the bits set by the IRR. The highest priority bits are selected and strobed into the corresponding bits of the ISR during the interrupt acknowledge cycle.

3.2.10.3 Interrupt Sequence

The events occuring during an interrupt:

- One or more IRR bits are set by a low-to-high transition or a high on the IR input lines.
- The 80130A evaluates these requests and sends INT (Interrupt, pin 29) to the 80186 if appropriate.
- When the 80130A receives the first interrupt acknowledge (status line S0/, S1/and S2/ all low) from the 80186 processor, the highest priority ISR bit is set. The corresponding edge detect latch in the 80130A is reset. The 80130A does not drive the address latch during this bus cycle but does acknowledge the cycle by generating LIR/ active for the IR input being acknowledged.
- The 80186 then starts a second interrupt acknowledge cycle. During this second cycle, at T1, the 80130A supplies the cascade address of the interrupting input and releases an 8-bit pointer onto the bus. The LIR/ output for the IR input being acknowledged is generated.

If no interrupt request is present when the second interrupt acknowledge cycle is stored (the interrupt request was too short) the 80130A issues an interrupt 7 pointer. The cascade address, the interrupt 7 pointer and the LIR/ will look like an interrupt level 7 (IR7) was requested.

3.2.10.4 Command Words

The 80130A accepts two types of command words generated by the 80186 processor. They are:

Initialization Command Words (ICWs): The 80130A and any slave controller in the system must be brought to a starting point by three, four, five or six initialization command words in succession.

Operation Command Words (OCWs): These are the command words that are sent to the 80130A for such operations as Interrupt Masking, End of Interrupt and Interrrupt Status. The operation command words can be written into the 80130A anytime after initialization.

3.2.10.5 Interrupt Initialization

Whenever a command is issued to the 80130A at address 0H with IOCS (80130A I/O CS/low), AD4 high and a write peripheral cycle, the data is interpreted as Initialization Command Word 1 (ICW1). ICW1 starts the initialization sequence which proceeds in the sequence shown:

- The edge sense circuits are reset. The first interrupt request following initialization must make a low-to-high transition or read a high level (depending on programming, see Section 3.2.10.8) to generate an interrupt.
- The interrupt mask register is cleared.
- Status read is sent to the IRR.
- The interrupt acknowledge cycle is reset and prepared for the first interrupt acknowledge cycle.
- All interrupts will be acknowledged by the LIR/ line going active. If ICW6 is written the interrupts will not be acknowledged.

3.2.10.6 Initialization Command Words 1 and 2

ICW1, ICW2, ICW4 is the minimum programming required by the 80130A PIC. The remaining control words ICW3, ICW5, and ICW6 are specified in ICW1 if their functions are needed. Once ICW1 is written the sequence is ICW2, ICW3, ICW4,

ICW5, ICW6. If either ICW3, ICW5 or ICW6 is not specified in ICW1, they are dropped from the sequence. The 80130A is ready to accept interrupts after the last initialization command word. ICW2 contains the bits T7-T3 of the vector supplied to the 80186 in the second interrupt acknowledge cycle.

The remaining bits 2 through 0 are determined by the interrupt level within the 80130A. The formats for ICW1 and ICW2 are as follows:

ICW1 Format

0	0	-	-	-	-	-	-	-	-	Unused, may be any value.
-	-	0	-	-	-	0	-	-	-	All slaves are non-local, no ICW6 read.
-	-	1	-	-	-	0	-	-	-	ICW6 to specify local slave inputs.
-	-	-	1	-	-	-	-	-	-	ICW1 indicator.
-	-	-	-	0	0	-	-	-	-	Edge triggered interrupt, no ICW5.
-	-	-	-	1	0	-	-	-	-	Level triggered interrupts determined by ICW5.
-	-	-	-	X	1	-	-	-	-	Level for interrupts determined by ICW5.
-	-	-	-	-	-	1	-	-	-	No slave units as IR inputs SNGL = 1.
-	-	-	-	-	-	0	-	-	-	One or more slave units as inputs SNGL = 0, ICW3 must be read.
-	-	-	-	-	-	-	1	-	-	ICW4 always needed.

ICW2 Format

T7	T6	T5	T4	T3	-	-	-	-	-	T3 through T7 are the five most significant bits of the vector byte supplied to the 80186.
-	-	-	-	-	X	X	X	-	-	Unused and may be any value.

3.2.10.7 Initialization Command Word 3

This word is only read when there are one or more slaves in the system and cascading is used. If there are one or more slaves, SNGL=0, in Initialization Command Word 1. ICW3 will load the eight bit slave identification register . A "1" bit is for each slave input in the bit position corresponding to the IR inputs.

ICW3 Format

1	-	-	-	-	-	-	-	-	-	-	IR7 has a slave.
0	-	-	-	-	-	-	-	-	-	-	IR7 does not have a slave.
-	1	-	-	-	-	-	-	-	-	-	IR6 has a slave.
-	0	-	-	-	-	-	-	-	-	-	IR6 does not have a slave.
-	-	1	-	-	-	-	-	-	-	-	IR5 has a slave.
-	-	0	-	-	-	-	-	-	-	-	IR5 does not have a slave.
-	-	-	1	-	-	-	-	-	-	-	IR4 has a slave.
-	-	-	0	-	-	-	-	-	-	-	IR4 does not have a slave.
-	-	-	-	1	-	-	-	-	-	-	IR3 has a slave.
-	-	-	-	0	-	-	-	-	-	-	IR3 does not have a slave.
-	-	-	-	-	1	-	-	-	-	-	IR2 has a slave.
-	-	-	-	-	0	-	-	-	-	-	IR2 does not have a slave.
-	-	-	-	-	-	1	-	-	-	-	IR1 has a slave.
-	-	-	-	-	-	0	-	-	-	-	IR1 does not have a slave.
-	-	-	-	-	-	-	1	-	-	-	IR0 has a slave.
-	-	-	-	-	-	-	0	-	-	-	IR0 does not have a slave.

3.2.10.8 Initialization Command Word 4

Initialization Command Word 4 is always required by the 80130A IWC4 selects between the Special Fully Nested or the Fully Nested modes. The format for ICW4 is shown below:

ICW4 Format

-	-	0	0	0	-	-	-	-	-	-	Unused.
-	-	-	-	-	0	-	-	-	-	-	Not fully Nested Mode.
-	-	-	-	-	1	-	-	-	-	-	Special Fully Nested Mode.
-	-	-	-	-	-	1	-	-	-	-	Buffered Mode.
-	-	-	-	-	-	-	1	-	-	-	Master.
-	-	-	-	-	-	-	-	0	-	-	Normal End of Interrupt.
-	-	-	-	-	-	-	-	-	1	-	80186 Mode.

3.2.10.9 Initialization Command Word 5

Initialization Command Word 5 is read only if it was specified in ICW1. ICW5 allows the option to individually select edge or level sensitive inputs to the IR inputs the 80130A. The format for ICW5 is shown below.

ICW5 Format	
1 - - - - - - - - -	IR7 is level triggered.
0 - - - - - - - - -	IR7 is edge triggered.
- 1 - - - - - - - -	IR6 is level triggered.
- 0 - - - - - - - -	IR6 is edge triggered.
- - 1 - - - - - - -	IR5 is level triggered.
- - 0 - - - - - - -	IR5 is edge triggered.
- - - 1 - - - - - -	IR4 is level triggered.
- - - 0 - - - - - -	IR4 is edge triggered.
- - - - 1 - - - - -	IR3 is level triggered.
- - - - 0 - - - - -	IR3 is edge triggered.
- - - - - 1 - - - -	IR2 is level triggered.
- - - - - 0 - - - -	IR2 is edge triggered.
- - - - - - 1 - - -	IR1 is level triggered.
- - - - - - 0 - - -	IR1 is edge triggered.
- - - - - - - 1 - -	IR0 is level triggered.
- - - - - - - 0 - -	IR0 is edge triggered.

3.2.10.10 Initialization Command Word 6

Initialization Command Word 6 is read only if it is specified in ICW1. ICW6 allows individual interrupt requests to be programmed as either local or non-local bus mode. If a bit in ICW6 allows individual interrupt request to be programmed as either local or non-local bus mode. If a bit in ICW6 is "1" then an acknowledgments of the corresponding IR input will output LIR/="0". If the same bit is "0" then an acknowledge of corresponding IR input will output LIR/='1". If ICW1 does not specify ICW6 all acknowledges for interrupts will generate LIR/="1". The format for ICW6 is:

ICW6 Format										
1	-	-	-	-	-	-	-	-	-	IR7 is local input.
0	-	-	-	-	-	-	-	-	-	IR7 is non-local input.
-	1	-	-	-	-	-	-	-	-	IR6 is local input.
-	0	-	-	-	-	-	-	-	-	IR6 is non-local input.
-	-	1	-	-	-	-	-	-	-	IR5 is local input.
-	-	0	-	-	-	-	-	-	-	IR5 is non-local input.
-	-	-	1	-	-	-	-	-	-	IR4 is local input.
-	-	-	0	-	-	-	-	-	-	IR4 is non-local input.
-	-	-	-	1	-	-	-	-	-	IR3 is local input.
-	-	-	-	0	-	-	-	-	-	IR3 is non-local input.
-	-	-	-	-	1	-	-	-	-	IR2 is local input.
-	-	-	-	-	0	-	-	-	-	IR2 is non-local input.
-	-	-	-	-	-	1	-	-	-	IR1 is local input.
-	-	-	-	-	-	0	-	-	-	IR1 is non-local input.
-	-	-	-	-	-	-	1	-	-	IR0 is local input.
-	-	-	-	-	-	-	0	-	-	IR0 is non-local input.

3.2.10.11 Operation Command Words (OCWs)

After the Initialization Command Words are programmed into the 80130A it is ready to accept interrupt request inputs. However during 80130A operation a selection of algorithms can, through the Operation Command Words, command the 80130A to operate in various modes.

3.2.10.12 Operation Control Word 1 (OCW1)

Operation Control Word 1 sets and clears the mask bits in the Interrupt Mask Register (IMR). These eight bits, M7 through M0, represent the eight mask bits. M=1 indicates the channel is masked (inhibited). M=0 indicates the channel is enabled. The format of Operation Control Word 1 is:

OCW1 Format

M7	M6	M5	M4	M3	M2	M1	M0	
1	-	-	-	-	-	-	-	IR7 is masked.
0	-	-	-	-	-	-	-	IR7 is enabled.
-	1	-	-	-	-	-	-	IR6 is masked.
-	0	-	-	-	-	-	-	IR6 is enabled.
-	-	1	-	-	-	-	-	IR5 is masked.
-	-	0	-	-	-	-	-	IR5 is enabled.
-	-	-	1	-	-	-	-	IR4 is masked.
-	-	-	0	-	-	-	-	IR4 is enabled.
-	-	-	-	1	-	-	-	IR3 is masked.
-	-	-	-	0	-	-	-	IR3 is enabled.
-	-	-	-	-	1	-	-	IR2 is masked.
-	-	-	-	-	0	-	-	IR2 is enabled.
-	-	-	-	-	-	1	-	IR1 is masked.
-	-	-	-	-	-	0	-	IR1 is enabled.
-	-	-	-	-	-	-	1	IR0 is masked.
-	-	-	-	-	-	-	0	IR0 is enabled.

3.2.10.13 Operation Control Word 2 (OCW2)

Operation Control Word 2 is used to terminate an interrupt level request. The format for OCW2 is as follows:

OCW2 Format

M7	M6	M5	M4	M3	M2	M1	M0	
0	1	1	-	-	-	-	-	Specific End of Interrupt.
-	-	-	0	0	-	-	-	Select OCW2.
-	-	-	-	-	0	0	0	End of Interrupt on IR0.
-	-	-	-	-	0	0	1	End of Interrupt on IR1.
-	-	-	-	-	0	1	0	End of Interrupt on IR2.
-	-	-	-	-	0	1	1	End of Interrupt on IR3.
-	-	-	-	-	1	0	0	End of Interrupt on IR4.
-	-	-	-	-	1	0	1	End of Interrupt on IR5.
-	-	-	-	-	1	1	0	End of Interrupt on IR6.
-	-	-	-	-	1	1	1	End of Interrupt on IR7.

3.2.10.14 End of Interrupt (EOI)

An In-Service (IS) bit can be reset by a command word that must be issued to the 80130A before returning from a service routine (EOI command). An EOI command must be issued twice, once for the master 80130A and once for the corresponding slave, if slaves are in use. A Specific End of Interrupt is the only EOI accepted by the 80130A and also the only designated function of OCW2. Part of this command includes the IS level to be reset.

3.2.10.15 Fully Nested Mode

This mode is entered after initialization unless another mode is programmed. The interrupt requests are ordered in priority from 0 thorugh 7, where 0 is the highest. When an interrupt is acknowledged, the highest priority request is determined and its vector placed on the bus. Additionally, a bit of the Interrupt Service Register (IS_{0-7}) is set. This bit remains set until the CPU issued an End of Interrupt (EOI) command immediately before returning from the service routine. While the IS bit is set, all further interrupts of the same of lower priority are inhibited, while higher levels will generate an interrupt.

3.2.10.16 Special Fully Nested Mode

This mode will be used in the case of a big system when one or more slaves are used in conjunction with the 80130A being the master controller, and priority must be conserved within each slave. In this case, the special fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal fully nested mode with the following exceptions.

a. When an interrupt request from a certain slave is in service, this slave is not locked out from the master's priority logic and further interrupt requests from high priority IR's within the slave will be recognized by the master and will initiate interrupt to the processor. In the normal nested mode, a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.

b. When exiting the Interrupt Service routine the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a specific End of Interrupt (EOI) command to the slave and then reading its IN Service register and checking for zero. If it is empty, a specific EOI can be sent to the master.

3.2.10.17 Edge/Level Triggered Modes

The 80130A has the compatible 8259A group pin selectable Edge or Level triggered mode of operation plus an additional individual pin Edge or Level triggered mode selection. If ICW5 is not specified in ICW1, then all IR inputs are either Edge Triggered or Level Triggered (See ICW1 format). If ICW5 is specified to be read, it contains a mask which determines individual IR input pin mode (See ICW5 format)

3.2.10.18 Local/Nonlocal Interrupts

The 80130A PIC has a special output, LIR, which when low, indicates an interrupt acknowledge cycle for an interrupt input with a corresponding bit set in ICW6. This output is provided to control the 8289 Bus Arbiter's SYSB/RESB pin. It avoids the need of requesting the system bus to acknowledge simple non slave interrupts or board resident (local) slave interrupts (i.e., 80P1). The PIC initialization must account for all interrupts that are local bus inputs by writing to ICW6 with the appropriate value. The default, if ICW6 is not written, is LIR-1 for interrupts.

In the as shipped (default) configuration of the iSBC 186/51S board, the 80130A will make LIR active in response to IR3 and IR4 active. The 8274 Multi-Protocol Serial Controller (U22), in the default configuration, can use only IR3 (8274 INTA/). If IR4 is used, PAL U31 must be reprogrammed.

3.2.10.19 Reading the Interrupt Control Starter

The input status of several internal registers in the PIC can be read to update the user information on the interrupt system. The following registers can be read via OCW3 (with the exception to IMR).

Interrupt Request Register (IRR): 8-bit register which contains the levels requesting an interrupt to be acknowledged.

In Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interupt command is issued.

Interrupt Mask Register (IMR): 8-bit register which contains the masked interrupt request lines.

The IRR can be read when, prior to the IORD cycle, a Read Register Command is issued with an OCW3 format (xxx1xxOB) written to I/O address OH (read IRR register on next read).

The ISR can be read when, prior to the IORD cycle, a Read Register Command is issued with an OCW3 format (xxx1xx1B) written to I/O address OH (read ISR register on next read).

There is no need to write an OCW3 before every status read operation, as long as the status read corresponds with the previous one; i.e., the 80130A remembers whether the IRR or ISR has been previously selected by the OCW3.

After initialization, the 80130A is set to read the IRR.

For reading the IMR, no OCW3 is needed. The IMR is read when accessing I/O address 2H.

3.2.10.20 Cascading

The 80130A and 80186 can be easily interconnected in a system of one 80130A being the master with up to eight PICs acting as slaves to handle up to 64 priority.

The slave interrupt outputs are connected to the 80130A IR inputs. When a slave request line is activated, the 80130A master will request a main interrupt system. On the second cycle of the interrupt acknowledge sequence, the 80130A will provide the

cascade address to the slave upon the AD8, 9 and 10 lines. The cascade address is available for latching utilizing the system's ALE strobe. The slave PIC will then return the pointer when it receives the second INTA strobe.

The 80130A always supplies the cascade address at ALE time of the second INTA cycle, and it will be the value of the Interrupt Level. It is obvious that each slave PIC in the system must follow a separate initialization sequence and be programmed to acknowledge a different cascade address. (See "Special Fully Nested Mode," Section 3.2.10.16.)

3.2.10.21 Timer Programming

See Table 3-17, page 3-104.

3.2.11 ETHERNET CONTROLLER PROGRAMMING

Section 3.2.11.1 describes the commands, data structures and techniques by which a host CPU, the 80186, controls and uses the 82586. The emphasis here is not on any particular action command, but rather on how the 82586 LCC is controlled.

The 82586 consists of two major internal processors: the Command Unit (CU) and the Receive Unit (RU). The control that the CPU exercises over them is indirect. Each unit accepts CPU commands during a ready state and although they are almost always ready, there may be a delay if the unit is busy responding to another request (internally generated). Both units can be viewed as multi-tasked units with non-preemption scheduling, although buffer switching tasks prempt the RU and CU.

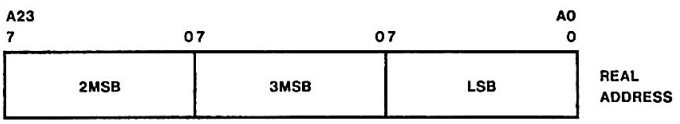
All control structures are memory resident and thus, all communications between the CPU and the 82586 takes place via shared memory structures. There is no I/O port access to the 82586.

3.2.11.1 Memory Addressing Formats

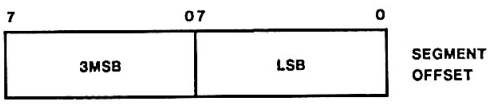
The 82586 accesses memory by 24-bit addresses. In the iSBC 186/51S application the upper four bits are ignored. There are two types of 24-bit addresses: real

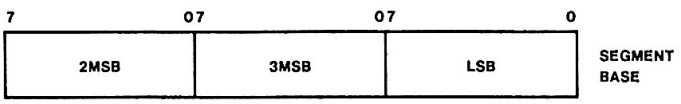
addresses and segmented addresses. A real address is a single 24-bit entity. It is used primarily to address transmit and receive data buffers. The other form is a segmented address that uses a 24-bit base and a 16-bit offset. The segmented address form is used for all Command Blocks, Buffer Descriptors, Frame Descriptors, and System Control Blocks. In general, only the offset portion of the addressed entry is specified in the block. The base for all offsets is the same (that of the SCB). The diagrams below detail the memory formats used. The LSB is the least significant byte of the address, 3MSB is the next most significant byte, 2MSB, if present, is the next most significant byte.

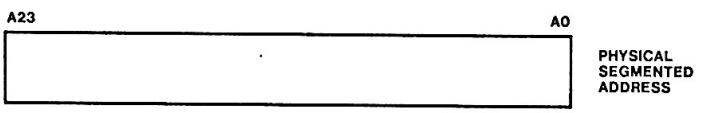
Physical (Real) data buffer addressing



Command structure addressing:







3.2.11.2 The System Control Block (SCB)

The SCB is a memory block that is shared by the CPU and 82586, and thereby forms the communication link between the CPU and the 82586. Such communication involves:

- o Commands issued by the CPU.
- o Status reporting from the 82586.

The CPU delivers Control commands to the 82586 by writing them into the SCB and asserting Channel Attention (CA). The 82586 will examine the command, perform whatever action is required and clear the command. Control commands perform four types of tasks:

- o Controlling the operation of the Command Unit (CU).
- o Controlling the reception of packets by the Receive Unit (RU)
- o Acknowledging events that caused an interrupt.
- o Resetting the chip.

The SCB controls the Command Unit by specifying the address of the Command Block List (CBL) and by starting, suspending, resuming or aborting execution of commands of the CBL. The SCB controls the Receive Unit by specifying the address of the Receive Packet Area (RPA), and by enabling, suspending, resuming or halting reception of frames.

The SCB is also used for reporting status to the host CPU. There are four types of status information contained in the SCB. The first describes the cause(s) of the currently pending interrupt (events). The second indicates the status of the Command Unit. The third indicates the status of the Receive Unit. The fourth

contains statistics collected by the 82586 related to receive frames, found to be corrupted.

There are four events saved by the 82586:

- o The completion of an action command by the CU.
- o The reception of a frame by the RU.
- o The Command Unit becoming not ready.
- o The Receive Unit becoming not ready.

The acknowledgement of events by the CPU is the only means by which interrupts are cleared. Note that if not all events are acknowledge by the Channel Attention (CA), then the Interrupt (INT) signal will be re-issued after processing the CA. Also, if a new event occurs while the interrupt is set, the interrupt is momentarily cleared in order to trigger edge-triggered input interrupt controllers.

The CPU commands the 82586 to examine the SCB via the Channel Attention line. This signal is trailing edge triggered and is latched by the 82586. The latch is cleared by the 82586 as part of the SCB examination process, prior to reading the SCB.

The format of the SCB is:

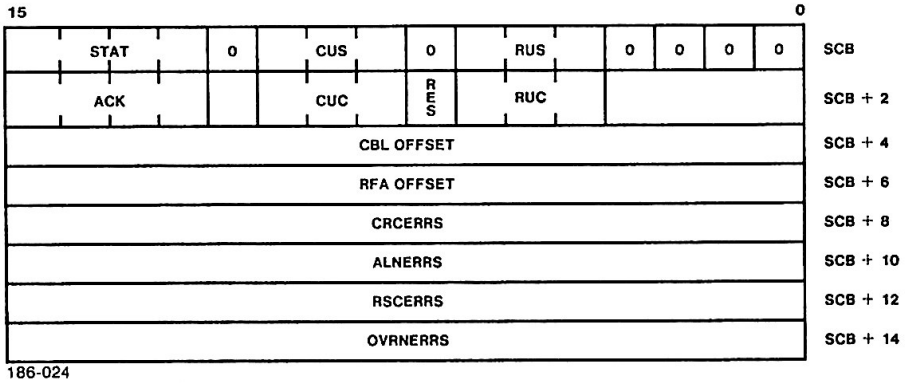


Table 3-11. SCB Block Definitions

STATUS –

Indicates the status of the 82586. This word is modified only by the 82586. Defined bits are:

Bit 15 CX – A command in the CBL having its 'I' (interrupt) bit set has been executed

Bit 14 PR – A packet has been received.

Bit 13 CNR – The command unit became not ready.

Bit 12 RNR – The receive unit became not ready.

Bits 8-10 CUS – (3 bits) The status of the command unit. Valid values are:

0 – Idle.
1 – Suspended.
2 – Ready.
3-7 – Unused.

Bits 4-6 RUS – (3 bits) this field contains the status of the Receive Unit. Valid Values are:

0 – Idle.
1 – Suspended.
2 – No Resources.
3 – Unused.
4 – Ready.
5-7 – Unused.

Command–

Specifies the action to be performed as a result of the CA. This word is set by the CPU and cleared by the 82586. Defined bits are:

Bit 15 ACK-CX – Acknowledges the command executed event.

Bit 14 ACK-PR – Acknowledges the packet received event.

Table 3-11. SCB Block Definitions (Cont'd.)

Bit 13 ACK-CNR– Acknowledges that the command unit became not ready.

Bit 12 ACK-RNR– Acknowledges that the receive unit became not ready.

Bit 8-10 CUC – (3 bits) this field contains the command to the unit Valid values are:

- 0 – NOP (does not alter current state of the unit)
- 1 – Start execution of the first command on the CBL. If a command is in execution, then complete it before starting the new CBL. The beginning of the CBL is in CBL OFFSET.
- 2 – Resume the operation of the command unit by executing the next command. This operation assumes that the command unit has been previously suspended.
- 3 – Suspend the execution of commands on CBL after execution of the current command is complete.
- 4 – Abort current command immediately.
- 5-7– Illegal for use. The effect will be exactly as NOP.

Bits 4-6 RUC – (3 bits) This field contains the command to the receive unit. Valid values are:

- 0 – NOP (does not alter current state of unit).
- 1 – Start reception of packets. If a packet is being received, then complete reception before starting. The beginning of the RFA (the RDL) is contained in RFA OFFSET.
- 2 – Resume receiving packets (only when in suspended state).
- 3 – Suspend packet receiving. If a packet is being received, then complete its reception before suspension.
- 4 – Abort receiver operation immediately.
- 5-7– Illegal for use. The effect will be exactly as NOP.

Table 3-11. SCB Block Definitions (Cont'd.)

Bit 7	RESET –	Reset chip (logically the same as hardware RESET).
CBL Offset	–	This 16-bit quantity specifies the offset portion of the address for the first command block on the CBL. It is accessed only if CUC = Start.
RFA OFFSET	–	This 16-bit quantity specifies the offset portion of the address for the Receive Packets Area (RPA) It is accessed only if RUC = Start.
CRCERRS Counter	–	This 16-bit quantity contains the number of misaligned packets discarded because of a CRC error. This counter is updated if needed, no matter what the state of the RU is.
ALNERRS Counter	–	This 16-bit quantity contains the number of misaligned packets discarded because of a CRC error. This counter is updated if needed in all RU states.
RSCERRS Counter	–	This 16-bit quantity contains the number of good packets discarded because there were no resources to receive them. Packets intended for a host whose RU is in the No Receive Resources state, fall into this category. This counter is updated only if the RU is in the No Resources state.
OVRNERRS Counter	–	This 16-bit quantity contains the number of packets that are known to be lost because of unavailability of the local system bus. If the traffic problem period lasts for more than one packet, the packets that follow the first one are lost without any indicator, and are not counted. This counter is updated, if needed in all RU states.

3.2.11.2.1 Error Counters Operation

- The CPU clears all error counters, prior to initiating the 82586. The 82586 updates these counters by reading them, adding one and writing back to their SCB positions. Multiple errors will result in all the relevant counters updating.

- The counters after reaching the value of FFFFH do not wrap around to zero. They will stay at this value, unless modified by the CPU.

- The 82586 will update all the statistical counters after every packet.

- The 82586 performs the read counter/increment/write counter operation without relinquishing the bus. This is done to ensure that no logical contention exists between the 82586 and the CPU. In a dual port memory configuration, the CPU should not perform any write operation to any counter unless the counter is in the FFFFH state. Otherwise, it is possible that the write operation will be overwritten by the 82586 that has recenlty read "old" information from the counter. Since the 82586 does not write to the counter when the FFFFH state is reached, the CPU may safely reset the counter.

3.2.11.2.2 Software Reset Operation

Upon reading a Reset bit in the SCB command word, the 82586 will:

- Terminate the Transmit and Receive processes.
- Ignore the remaining SCB command field.
- Clear the SBC command word.
- Reset the chip.

After the 82586 has cleared the SCB command word, the reset effectively starts. Note that INT is not raised. The CPU must wait at least 10 system clocks before issuing the CA to the 82586, to trigger the initialization procedure.

3.2.11.2.3 Semantics of Control Commands

Control Commands are submitted independently to the RU and CU. The explanation below applies for both RU and CU control commands.

The commands are treated by the 82586 in two phases. The first phase is named CONTROL COMMAND ACCEPTANCE. Its termination is indicated by the 82586 clearing the SCB command word. Acceptance is complete after the 82586 responded to the CPU's request, read the command from SCB command word and performed the required activities, which depend on the state of the CU or RU.

The second phase is named CONTROL COMMAND EXECUTION, and is performed as soon as the current CU or RU activity (at CB or PD level) is finished. For the CU, it happens when the Command Block currently in execution is completed. For the RU, it happens when the packet currently in reception has ended.

Both the CU and RU have a pointer to the next CB (for CU) or RPD (for RU). NEXT CB points to the Command Block to be executed after the current CB is completed. NEXT RPD points to the RPD to be set up after the present packet is received.

3.2.11.2.4 Control Command Effects

Start – This command specifies the list of CBs or RPDs. NEXT CB or NEXT RPD pointer is always updated. If the unit is not active during acceptance (i.e., the CU is not executing CBs or the RU is not receiving a packet), the next CB or RPD will immediately be set up. In this case, the acceptance and execution phases overlap. If the unit is active during acceptance, the next CB or RPD will be set up at the end of the current activity (execution phase). In all cases, the next state of the units is READY.

Abort – At acceptance time, this command causes the immediate termination of the CU or RU activities. End of execution is signalled by the CU or RU entering their idle state.

Suspend – This command is ignored if the unit is not READY, at acceptance time. If the unit is READY, the present activity is completed (CB execution for CU and packet reception for RU) and the unit becomes suspended.

Resume – This command is ignored if the unit is not SUSPENDED. If during acceptance, the unit is not active (CB execution for CU, packet reception for RU) then NEXT CB or NEXT RPD is set up. Otherwise, the NEXT CB or NEXT RPD is set up at the end of the current activity. In any case, after execution, the new state of CU or RU is READY.

At the end of the activity (CB completion or reception of a packet completed), the CU or RU assesses its situation based upon :E: and :S: bit status. If "EL" is set, the last CB or RPD was exhausted. The CU becomes IDLE or the RU enters its No Resources state, regardless of any other factor. If "S" is set, the unit becomes suspended.

"Requests" remembered from acceptance time are as follows:

- o If a Suspend is requested, the unit becomes SUSPENDED.
- o If a Start is requested, the unit enters its READY state and CB or RPD setup follows.
- o If no request is pending, CB or RPD set up follows per Command Block List or Receive Frame List.

3.2.11.2.5 Rules for Using Control Commands

Handshake

The CPU write the control command to the SCB command word and causes a falling edge of CA input.

The 82586, after a finite but undefined number of clocks, recognizes the CA transition and performs its control command acceptance procedure. At the end of the sequence, the 82586 clears the whole SCB command word and places current CU and RU status into the SCB.

At this time, the CPU is allowed to issue the next control command to the 82586.

A new accepted control command cancels a previous control command that was accepted and awaits execution. (Note: A NOP control command does not cancel previous commands. This is provided to allow acknowledging interrupts without disturbing the CU and RU operation.

Normal Operation

The CPU is notified that the control command was accepted by the 82586. This notification is signalled by the 82586 clearing the SCB command word.

The execution of control commands may be deferred because of the CU and RU being active (CB execution or packet reception) at command acceptance time.

When the control command execution is completed the new status of the CU and RU is reported.

The only state transitions that are specifically signalled, with interrupt to the CPU, are RU and CU becoming not READY. Interrupt also happens at the completion of a CB (with 1 bit set) and after completing reception of a packet.

3.2.11.3 The Command Unit

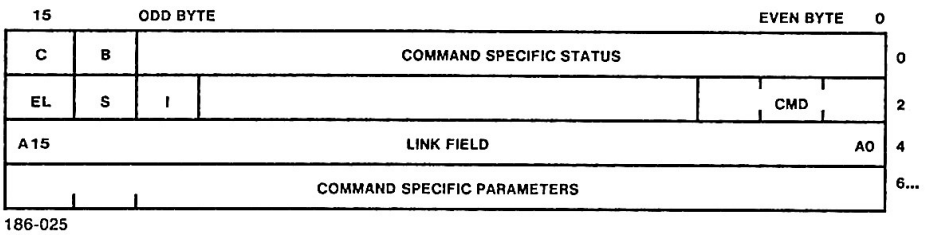
The CU is responsible for handling commands from the CPU. These commands fall into two categories: control and action. This section is concerned primarily with control commands and the generic class of action commands. Action commands are discussed in detail in Section 3.2.11.9.

Control commands are the means by which the CPU controls the CU's execution of action commands. Action commands are located in Command Block (CB) which are then linked together to form the Command Block List (CBL). The CBL may contain one or more CBs. The last CB is indicated by the End List (EL) bit in the CB being a one. The CU starts at the beginning of the CBL and executes the commands, one at a time, until the CB where EL = 1.

3.2.11.3.1 Command Blocks

Action commands are organized in blocks (CBs). The beginning of the CBL is defined by the CBL OFFSET in the SCB and its end is indicated by the EL bit (EL = 1) in the last CB.

The generalized form of command block is:



where:

STATUS – This 14-bit field contains the command results it is set at the same time as the C bit. It is not valid until C = 1.

Bit 13 – Indicates that the command was executed without error. If one, then no error occurred (command executed 0). If zero, then an error did occur and the remaining bits should be consulted to discover what the problem was.

Bit 12 – If set, it indicates that the command was abnormally terminated due to CU Abort control command. If one, then the command was aborted and if necessary, it should be repeated. If bit 12 is zero, the command was not aborted.

LINK FIELD – A 16-bit pointer to the next command block.

EL – If set, this bit indicates that this command block is the last on the CBL.

EL – If set, this bit indicates that this command block is the last on the CBL.

S – If set to 1, the CU is suspended upon completion of this CB.

I – If set to 1, the 82586 will generate an interrupt after execution of the command is completed. If I is not set to one, the CX bit will not be set.

CMD – A 3-bit field that specifies the op code of the command. See Section 3.2.11.9 of this manual.

Bits 4-12 – Reserved.

C – This bit indicates the execution status of the command. The CPU initially sets it to zero when the Command Block is placed on the CBL. Following a command execution, the 82586 will set it to one.

B – This bit indicates that the 82586 is currently executing this command. It is initially set to zero by the CPU. The 82586 sets it to one when execution begins and to zero when execution is complete.
NOTE: The C and B bits are modified in one operation.

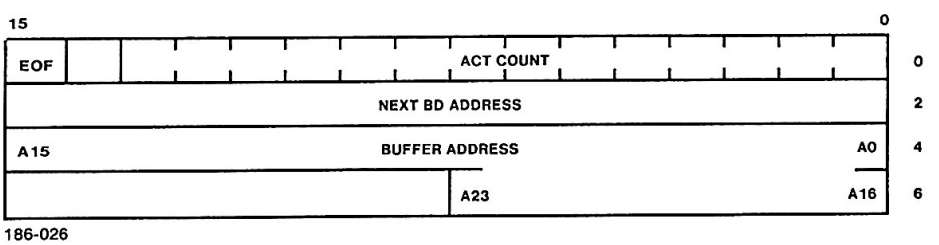
COMMAND SPECIFIC PARAMETERS – This is a variable length field that contains parameters for and/or results from the command. Its length and contents are command dependent. For further details see Section 3.2.11.9 of this manual.

Command Blocks are chained together to form the CBL. When searching the CBL after an interrupt, the CPU can remove any block with C = 1, since execution is complete. The forward link in the last CB may be used to form a cyclic list.

3.2.11.3.2 Transmit Buffer Descriptor

The transmit command accesses user data contained in buffers for Transmit operations. Each buffer is described by a Transmit Buffer Descriptor (TBD). TBDs are used with Transmit commands to contain user data that is to be sent. Each command may contain zero or more TBDs. The TBDs are linked together to form a packet. They are automatically prefetched by the CU as required.

The TBD has the following format:



where:

EOF – This bit indicates that this TBD is the last associated with the packet being transmitted. Set by the CPU before transmitting.

ACT–COUNT – This 14 bit quantity specifies the number of bytes in the buffer that holds information for the current buffer. It is set by the CPU before transmit.

NEXT BD ADDRESS– The offset portion of the address of the next TBD on the list. It is meaningless if EOF = 1.

BUFFER ADDRESS – The starting address of the memory area that contains the data to be sent. This is a 24-bit physical address. In WORD mode the buffer address must be even.

3.2.11.3.3 Command Unit Control

The CU may be in one of three major states during normal operation. These states are:

IDLE – In this state the CU has no action commands to execute. It will still respond to control commands. The CU is initialized to IDLE state.

SUSPENDED – This state is similiar to IDLE, except that the CU may become READY by a Resume command. It remembers the state of the CBL list. It comes to this state only via a Suspend control command or by executing a CB with S =1.

READY – In this state, the CU has commands on the CBL and is executing them.

The following are the events that may cause the CU to change state:

a. All Control Commands. The control commands are:

NOP – This command is ignored by the CU.

SUSPEND – This command suspends operation of the CU when the currently executing command is complete.

RESUME – This command returns the CU to the READY state from the SUSPENDED STATE.

START – This command gives the CU a new CBL to work on.

ABORT – This command stops the CU immediately. Execution of commands is stopped.

b. Action command (whose CB has S= 1) executed.

c. The end of the CBL is reached.

Multiple events may occur concurrently.

SET UP CB means start processing the next command in the queue.

REQUEST SUSPEND means the suspend will be executed as soon as the command currently being executed is done.

Most of the transitions do not cause interrupts. In actual operation, CX interrupts will be the most common. When the CPU receive an interrupt it examines the CBL and removes all CBs with C =1 (there may be more than one). The CPU should always keep the pointer to the first unexecuted CB.

After the initialization process is complete (see Section 3.2.11.7) the CU will issue both a command executed (CX) and a CU not ready interrupt. The CPU must be expecting such interrupts at the end of the initialization process.

Table 3-12 shows the CU activities at the end of the control command execution time.

3.2.11.4 The Receive Unit

The Receive Unit (RU) handles all activities related to packet reception. It operates independently of the CU although it does use the CU to communicate with the CPU. It manages a pool of free space called the Receive Packet Area (RPA) that consists of two lists: Received Packet List (RPL) and Free Packet List (FPL). The SCB points to the RPL and the last packet in the RPL points to the FPL.

The Free Packet List (FFL) consists of two lists. The first is a list of free Receive Packet Descriptors (RPD), called the Receive Descriptor List (RDL). The second is a list of free buffers called the Free Buffer List (FBL) with each described by Receive Buffer Descriptor (RBD). The Root of the FBL is the first RFD on the RDL (Figure 3-19).

The address of the RFA (the first RFD on the RDL) is given to the RU by the CPU issuing a SCB. One RFD is used for each received packet and as many RBDs (actually the buffers associated with each) as are required to contain the packet.

When either list is exhausted the RU notifies the CPU and enters the No Resources state.

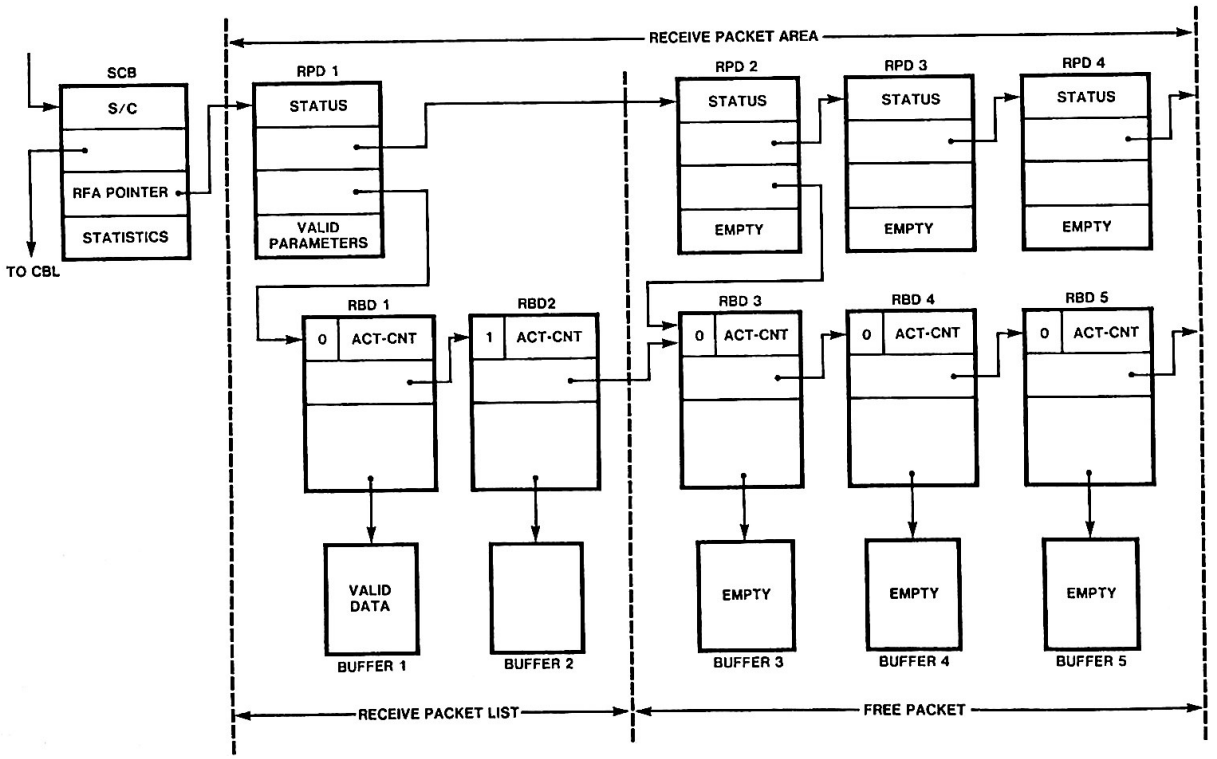


Figure 3-19. Receive Frame Area

Table 3-12. CU Activities Performed at the End of Execution

EL Bit	S Bit	Request	Next State	Action
0	0	None	Ready	Set UP CB
0	0	Suspend	Suspended	CNR Interrupt
0	1	None	Suspended	CNR Interrupt
0	1	Suspend	Suspended	CNR Interrupt
1	0	None	Idle	CNR, CX Interrupt
1	0	Suspend	Idle	CNR, CX Interrupt
1	1	None	Idle	CNR, CX Interrupt
1	1	Suspend	Idle	CNR, CX Interrupt

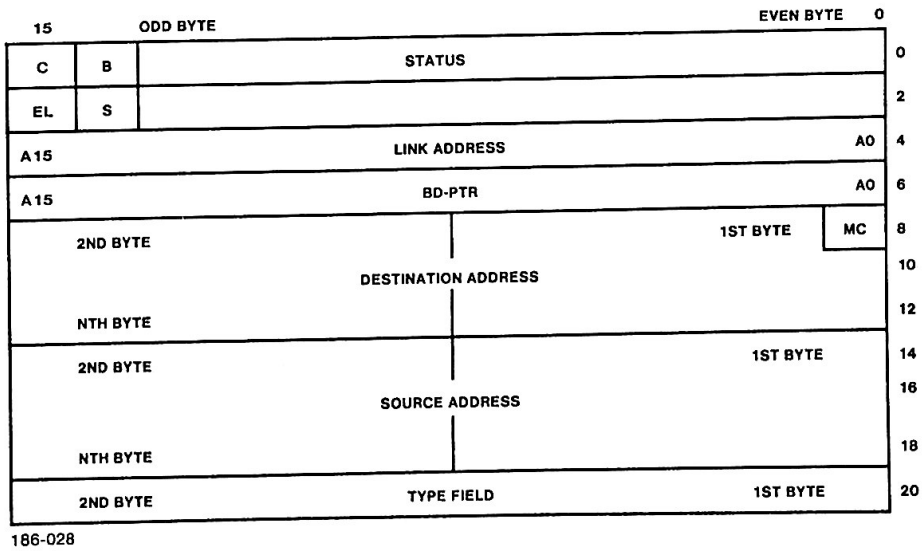
NOTES:

1. After a CB with I-bit set is completed, CX interrupt is generated.
2. Since the transition from the READY state to the READY state via the START command is smoothly performed, no interrupt, related to state transition, is generated and no action is required at the end of Action Command Execution.

3.2.11.4.1 The Receive Packet Descriptor

Each received packet is described by one Received Packet Descriptor. The RPD used is the one at the head of the RDL.

The format of the receive packet descriptor is:



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where:

STATUS – The results of the receive packet descriptor operation. Defined bits are:

Bit 13	–	Packet received without errors
Bit 12	–	Reserved - Unused
Bit 11	–	CRC error in an aligned packet
Bit 10	–	Alignment error (CRC error in misaligned packet)
Bit 9	–	Ran out of buffer space
Bit 8	–	DMA Overrun
Bit 7	–	Packet too short
Bit 6	–	No EOF flag (for Bitstuffing only)
Bit 0-5	–	Reserved - Unused

RPD's with Bit 13 not equal I will occur only if the SAVE-BAD PACKET configuration option is selected. Otherwise all packets with errors will be discarded, although statistics will be kept on them.

Link Address – The 16-bit pointer to the next Receive Packet Descriptor. The Link Address of the last packet can be used to form a cyclic list.

EL – If set, this bit indicates that this RPD is the last one on the RDL.

S – If set, suspend the RU after receiving this packet.

C – This bit indicates the completion of packet reception. It is set by the 82586.

B – This bit indicates that the 82586 is currently receiving this packet or that the 82586 is ready to receive the packet. It is initially set to zero by the CPU. The 82586 sets it to one when reception set up begins, and to zero upon completion. The C and B bits are set in one operation.

BD-PTR – The offset portion of the address of the first RBD containing packet data. BD-PTR = 0FFFFH indicates no RBD at all.

MC – Multicast bit.

DESTINATION-ADDRESS – The contents of the destination address of the receive packet. The field is 0 to 6 bytes long.

SOURCE ADDRESS – The contents of the source address field of the received packet. It is 0 to 6 bytes long.

Type Field – The contents of the type field of the received packet. It is 2 bytes long.

NOTES:

1. The last 4 fields will not be used when the 82586 is configured to locate address/control in the data buffers (AC-LOC=1).

2. The last four fields are packed, i.e., one field immediately follows the next.

The receive buffers can be of different lengths. The 82586 will place no more bytes into a buffer than is indicated in the associated RBD. The 82586 will prefetch the next RBD in time to use it.

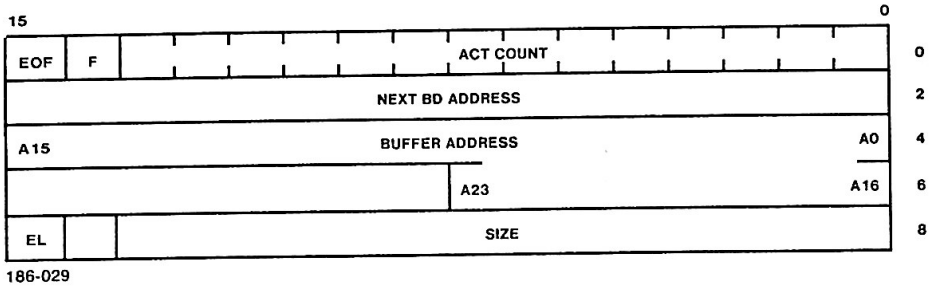
Before starting the RU, the CPU must place the pointer to the FBL in BD-PTR field of the first RPD. All remaining BD-PTR fields for the subsequent RPDs should be FFFFH.

If the Receive Packet Descriptor and the associated receive buffers are not reused (packet is well received of the 82586 works in a mode where it saves bad packets), the 82586 writes to the BD-PTR field of the next RPD the address pointer of the next free RBD.

3.2.11.4.2 Receive Buffer Descriptor (RBD)

The information field of a packet is not part of a RPD, but is accessed with a special pointer to a separate block in order to provide the flexibility of separating the control from the information. The information field of a packet is placed in a

set of buffers that are chained by a sequence of Buffer Descriptors. A RPD points to the first RBD, and the last RBD is flagged with an EOF set to one. The format of the receive buffer descriptor is as follows:



where:

EOF – Indicates that this is the last buffer related to the packet. It is cleared by the CPU before starting the RU and written by the 82586 at the end of reception of the packet.

F – Indicates that this buffer has already been used. The Actual Count has no meaning unless the F bit equals one. This bit is cleared by the CPU before starting the RU, and set by the 82586 after the associated buffer has already been used.

ACT COUNT – This 14-bit quantity indicates that the number of meaningful bytes in the buffer. It is cleared by the CPU before starting the RU and written by the 82586 after the associated buffer has already been used. In general, after the buffer is full. Actual Count value equals the size field of the same buffer. For the last buffer packet, Actual Count maybe less than the buffer size. NOTE: If Actual Count is odd (in word mode), invalid data will be written to the 82586 into the high byte of the last word.

NEXT BD ADDRESS – The offset portion of the address of the next RBD on the list. It is meaningless if EL = 1.

BUFFER ADDRESS – The starting address of the memory area that contains the data that was received. This is a 24-bit physical address. In word mode, the buffer address must be even.

EL – Indicates that the associated buffer to this RBD is last in the FBL.

SIZE – This 14-bit quantity indicates the size, in bytes, of the associated buffer. In word mode the quantity must be even.

3.2.11.4.3 Receive Unit Control

The RU may be one of four states.

These states are:

IDLE – In this state the RU does not respond to packets on the serial link and does not modify any data structures. The RU is initialized to this state.

SUSPENDED – This state is similiar to IDLE, except that the RU may become READY by means of a Resume command. It remembers the state of the RPA lists. It comes to this state via a SUSPEND control command or use of a RPD with S = 1.

NO RESOURCES – In this state the RU is looking for packets on the serial link, but has no buffers to store them in. It will keep statistics on how many packets were lost.

READY – In this state, the RU is looking for packets and has buffers in which to store them.

In each of these states, the RU may or may not be receiving a packet. A situation in which a packet is being received, called "RU Actively Receiving." If the RU is

READY and Actively Receiving, the packet is being stored in RPA buffers. If the RU is not READY, (IDLE, SUSPENDED or NO RESOURCES), the packet is discarded. The RU still maintains statistics on CRC, Alignment or Overrun error for discarded packets, although the packets themselves are lost.

The following are the events that may cause the RU to change state:

All Control Commands. The control commands are:

NOP – This command is ignored by the RU.

SUSPEND – This command suspends operation of the RU when the packet reception is completed.

RESUME – This command causes RU transition from SUSPENDED state to READY state.

START – This command gives the RU a new RPA to work on. The RU is exited to READY state.

ABORT – This command stops the RU immediately. Reception of any packet is stopped and the CU goes into the IDLE state.

A packet is received using a RPD with S = 1.

The end of the RDL or FBL is reached.

Set UP RPD means" Prepare the next RPD for packet reception.

Most transitions do not cause interrupts. Most interrupts are caused by packets being received. When the CPU gets a PR interrupt, it should scan down the RDL, removing all RPDs where C = 1. There may be more than one RPD. The CPU should keep a pointer to the head of the RDL.

RU Not Ready interrupt, might be caused by a control command issued by the CPU to the RU, reception of a packet using a RPD with S = 1, or to the exhaustion of either (or both) the RDL or FBL.

The reason for RNR interrupt may be identified by CPU, knowing it has issued a control command and by testing the S and EL bits of the last used RPD.

Table 3-13 shows the RU activities at control command execution time.

Regardless of its state, the RU looks for start requests at the end of a receive packet. This guarantees that packets are either housed in the old RPA or entirely in the new RPA. There is a sharp transition from the old RPA to the new RPA, that takes place at the end of the receive packet.

Note that the process of starting the RU takes time. During this time, receive packets may be lost due to a temporary lack of memory resources. This situation may arise, even if the previous RPA has enough resources to contain the incoming packet.

Table 3-13. RU Activities Performed at the End of Execution

EL Bit	S Bit	Request	Next State	Action
0	0	None	Ready	Set up RPD
0	0	Suspend	Suspended	RNR Interrupt
0	0	Start	Ready	Set Up RPD
0	1	None	Suspended	RNR Interrupt
0	1	Suspend	Suspended	RNR Interrupt
0	1	Start	Suspended	RNR Interrupt
1	0	None	No Resources	RNR Interrupt
1	0	Suspend	No Resources	RNR Interrupt
1	0	Start	Ready	Set Up RPD
1	1	None	Idle	RNR Interrupt
1	1	Suspend	Idle	RNR Interrupt
1	1	Start	Ready	Set Up RPD

NOTE: After a packet is received, FR interrupt is generated.

Depending on the 82586 internal state, the RSCERR or OVRNERR counters in SBC will be updated. CRCERR and ALNERR counters will be updated as usual.

3.2.11.5 Interrupt Operation

The INT pin is used to notify the CPU about one or more of the following events.

- o A command in CB with its I-bit set was executed (CS interrupt).
- o A packet was received (PR interrupt).
- o The CU became Not Ready (CNR interrupt).
- o The RU became Not Ready (RNR interrupt).

3.2.11.5.1 Interrupt Request Sequence

Once an event requiring an interrupt has occurred, the following sequence is performed by the 82586:

a. INT pin is set to its low level (inactive).

b. The status word in SCB is written, denoting the source of the interrupt (CX, PR, CNR or RNR interrupt), together with the states of the CU and RU.

c. INT pin is raised (set to active).

3.2.11.5.2 Interrupt Servicing by the CPU

Upon detecting a rising edge on the INT pin, the CPU may perform its interrupt service routine, as follows:

a. Save registers.

b. Wait until the SCB command word is All Zero.

c. Read SCB STATUS field.

d. Determine the cause(s) of the interrupt and the states of the CU and RU.

e. Process each interrupt cause and determine the next control commands for the CU and RU.

f. Write Interrupt Acknowledge bits to the processed interrupt requests together with the next control commands for CU and RU.

g. Issue a CA falling edge to the 82586.

h. Restore registers and exit interrupt routine.

3.2.11.5.3 82586 Response to CA

Upon detecting a falling edge on its CA input, the 82586 performs the CA acceptance sequence, as follows:

a. Determine which interrupt requests were acknowledged by the CPU. For each of them clear the corresponding interrrupt request bit in SCB status word.

b. Perform the control command acceptance procedure, as described in C.3 (for the CU) and D.3 (for the RU).

c. The INT pin is set LOW.

d. Write the SBC status word indicating the unacknowledged interrupt request, and newly generated interrupt requests, together with CU and RU states.

e. If any interrupt requests bit is active, set the INT pin to HIGH.

3.2.11.5.4 Initialization Procedure

82586 Actions

o After Reset (either hardware or software reset), INT pin is set to its low level (inactive).

- The 82586 waits for a CA high to low transition.

- When this happens, the initialization procedure is performed. Upon completion, CX (Command Executed) and CNR (CU became Not Ready), interrupts are written to SCB status word, together with the status of CU and RU (both are idle).

- The INT pin is then set to HIGH

CPU Actions

- CPU should expect interrupts as past of the 82586 initialization procedure.

- It writes the control commands for the CU and RU (typically STARTing both) and acknoweldges the CX and CNR interrupts.

- It issues a CA to the 82586 and the INT/CA handshake mechanism keeps rolling on by itself.

3.2.11.6 Interaction Between Control and Action Commands

3.2.11.6.1 82586 Channel Attention (CA) Timing

The CU is responsible for control command acceptance, following the trailing edge on CA input. The CU will first finish all its higher priority activities and only then accept the control commands.

Higher priority CU activities that delay CA acceptance are:

- Transmit BD prefetch.
- Transmit buffer switching.
- Current CB command completion.

The 82586 will accept a CA prior to the set up of the next CB in the CBL.

The CU recognizes an RU control command and notifies the RU. The RU will first finish all its higher priority activities, and only then accept the control command.

Higher priority RU activities that delay CA acceptance are:

- o Receive BD prefetch.
- o Receive buffer switching.
- o Receive end of packet processing.

Only after the CU and RU have accepted the control command, the SCB command word is cleared. At that time the CPU may issue the next CA to the 82586.

Internally to the 82586, the CA trailing edge is detected and latched. Prior to reading the SCB control command, the 82586 clears the latch. A new CA, given to the 82586 before the SCB command word is cleared, may be lost due to its being cleared before serviced. The user must refrain from such violations.

The 82586 does not wait until for reception or transmission to end in order to process a CA. The SCB related operations will be carried out on an interleaved basis with the transmission or reception process.

3.2.11.6.2 Critical Regions in the Interface to the CPU

Common Bus Operation

When the 82586 and the CPU reside on the same system bus, the bus acquisition and release is governed by the HOLD/HLDA protocol. This scheme ensures that only one bus master owns the bus at a time.

The 82586 performs its bus accesses to a descriptor in memory without relinquishing the bus. This results in a certain number of system clocks where the system bus is owned by the 82586, but no bus activity happens.

The only way for the CPU to force the 82586 off the bus during descriptor processing, is by dropping HLDA. In this case, the CPU and any other master peripheral must refrain from modifying 82586 memory control structure.

The affected descriptors are:

- o Command Blocks.
- o Receive Packet Descriptors.
- o Transmit Buffer Descriptors.
- o Receive Buffer Descriptors.
- o System Control Block.

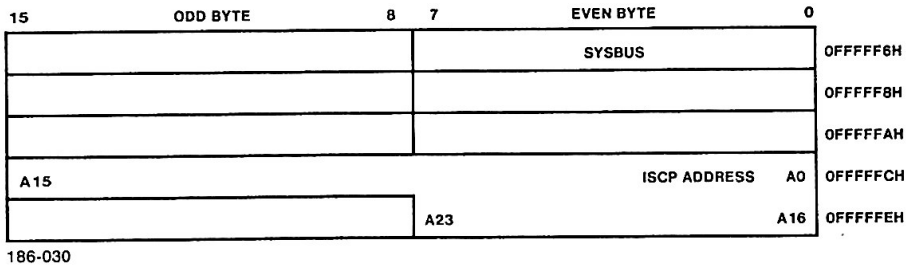
3.2.11.7 Initialization and Configuration

The 82586 accesses the "Initialization Root" as part of the initialization sequence, begun after CA is asserted for the first time following a RESET. The Initialization Root consists of two data structures addressed via two pointers: the System Configuration Pointer (SCP) and the Intermediate System Configuration Pointer (ISCP).

The primary purpose of this process, in addition to simply getting the 82586 into a stable state, is to locate the SCB and thus define the 64K Byte page in which all command/control structures are located.

3.2.11.7.1 The System Configuration Pointer (SCP)

The SCP begins at a location 0FFFF6H and is the only fixed address data structure in an 82586 system. Its purpose is to specify the width of the data bus used by the 82586 (8 or 16 bits), as well as the location of the ISCP. The SCP for the 82586 shares the location 0FFFF6H with the SCPs of all other master peripherals. The format of the SCP is:



where:

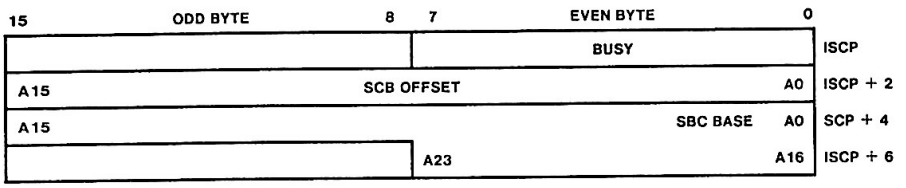
SYSBUS – Specifies whether the system data bus available to the 82586 is 8-bits or 16-bits wide. A "1" indicates 8-bits and a "0" indicates a 16-bits. During the first read operation from the SCP, the 82586 assumes a byte wide bus, reading the SYSBUS byte. The bus width goes into effect immediately after SYSBUS is read.

ISCP ADDRESS – A 24-bit quantity that is the physical address of the ISCP.

3.2.11.7.2 The Intermediate System Configuration Pointer (ISCP)

The ISCP specifies the location of the SCB. Usually, all Master peripherals in a system share the same ISCP address. The SCP will often be in ROM with the ISCP in RAM. The CPU will load the address of the SCB (or an equivalent data structure) for each Master peripheral into the ISCP and assert the peripheral's CA. The 82586 now begins initialization procedure to fetch the address of the SCB via the SCP and ISCP.

The base address of the SCB is also base address of all Command Blocks, Packet Descriptors and Buffer Descriptors (but not buffers) in the system. All such data structures must exist in a 64K Byte segment. The format of the ISCP is:



where:

BUSY – Indicates that the 82586 is being initialized. It is set to 01H by the CPU before its first CA to the 82586. It is cleared by the 82586 after the SCB base and offset are read. Note that the most significant byte of the first word of the ISCP is not modified when BUSY is cleared.

SCB OFFSET – This 16-bit quantity specifies the offset portion of the address of the SCB.

SCB BASE – This 24-bit quantity specifies the base portion of the address of the SCB. The base of SCB is also the base of all 82586 Command Blocks, Packet Descriptors and Buffer Descriptors.

NOTE: All descriptors (segment addresses) must start at even addresses in word mode.

3.2.11.7.3 Initialization Procedure

The CPU sets up the SCP, ISCP, and the SCB structures. It also sets BUSY to 01H.The initialization procedure is started by the CA following a RESET. This CA causes the 82586 to access the SCP at locations 0FFFF6H (see Figure 3-20). The SYSBUS byte is fetched in byte mode. Once the bus width is determined, all further memory transfers will be at the specified bus width. After the SCP is addressed, the 82586 fetches the ISCP. The 82586 saves the base of the SCB (that is, the base of all control blocks), as well as the SCB address. It clears busy, sets CS=1 and CNR=1 in the SCB, clears the SCB Command word, signals an interrupt to the CPU and waits for a CA.

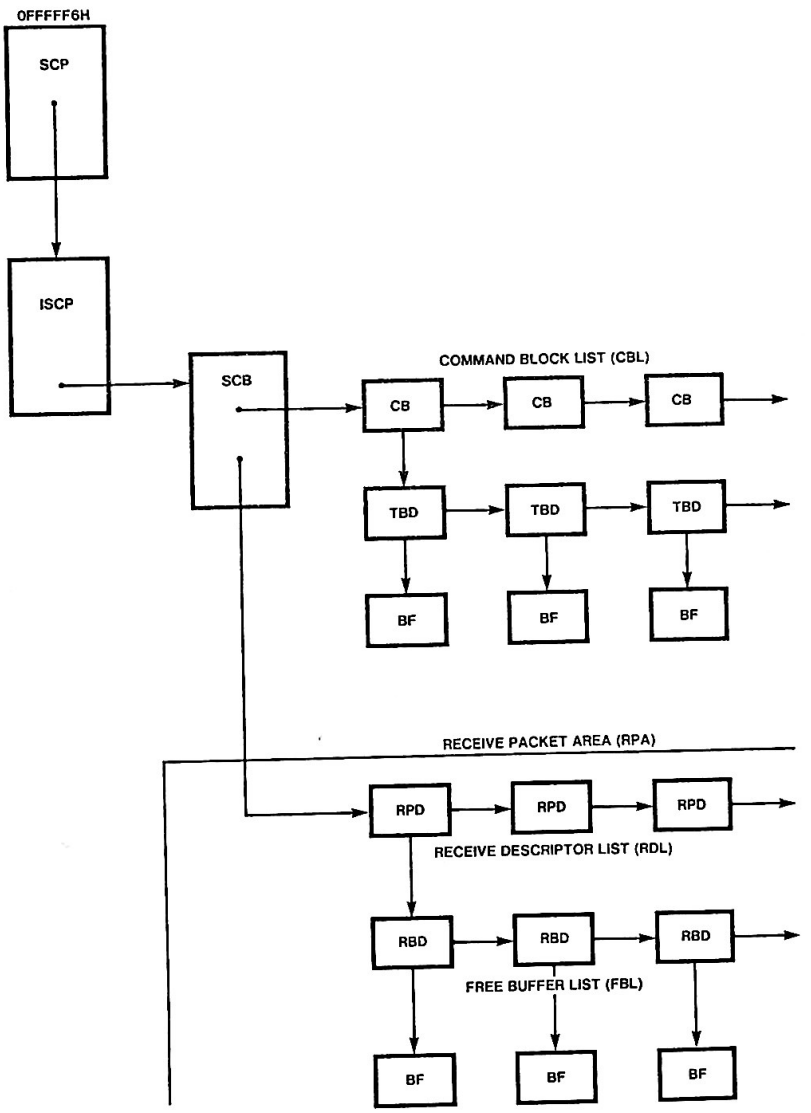


Figure 3-20. The Shared 82586/CPU Memory Structure

The RESET configures the 82586 prior to the CA, to the operational mode compatible with the Ethernet standard. Only Broadcast Address is accepted by the 82586 until an Individual Address is set up. If there is a need to change some parameters, this can be done with a CONFIGURE Command.

3.2.11.8 Configuration

Operation parameters are loaded into the 82586 via the configure command (see Section 3.2.11.10).

FIFO Limit

Specifies the point in the FIFO at which the 82586 request the bus in order to transfer data to/from its internal FIFO from/to memory.

SRDY/ARDY

Selects between synchronous ready function and asynchronous ready function of the SRDY/ARDY pin.

0 ARDY – Asynchronous Ready, i.e. The Ready signal is internally synchronized by the 82586. This adds one wait state to the 82586 bus cycle.

1 SRDY – Synchronous Ready, i.e. The Ready signal is externally synchronized.

Save-Bad Packet

Specifies whether errored packets (CRC error, Alignment error, etc.) are to be discarded or saved. 0- discard, 1 - save. In Save Bad-Packet mode, the Receive Packet Descriptor, as well as the Receive Buffer Discriptors and Receive Buffers are NOT reused for the next packet. In the complementary mode, all the descriptors and buffers used for bad packets, will be reused thus, not leaving any information about the lost packet except for statistical tallies update.

Address Length

Determines the length in bytes, of the address that the 82586 refers to. This includes Source, Destination, Multicast, or Broadcast Addresses,

Address/Control Field Location

0 – Address and control type are located in consecutive bytes in the descriptor.

1 – The whole packet is located in the data buffers. Source address insertion by the transmitting the 82586, is disabled.

INT-Loopback

When set, the 82586 disconnects itself from the serial wire and logically connects TxD to RxD and TxC to TRC. TxC must still be supplied by the user. Internally, TxC is divided by 4. This slows down the serial bit rate sufficiently to enable 82586 operation in full duplex. This will alter the effective values to all configure command parameters that are defined in terms of TxC. Note, the INT-Loopback bit set, at the same time with EXT-Loopback, cause the 82586 to operate in Internal Loopback Mode.

EXT-Loopback

The 82586 will receive and transmit simultaneously, at full rate, a packet limited to 18 bytes (including the Packet Check Sequence). This allows checking of external hardware as well as the serial link to the transceiver. For Ethernet transceivers, since the transmitted data is fed back via the receive pair practically nothing has to be done to perform External Loopback. For other transceiver types, the user is responsible for external transmit-receive interconnection.

Note: Internal Loopback bit overrides External Loopback bit.

Linear Priority

These bits define the amount of delay (expressed in Slot Time period units) that a station will withhold itself from transmission after the Interpacket Spacing.

For Linear Priority greater than zero, the 82586 will check the Carrier Sense of the time out completion. If the station senses carrier, it assumes that higher priority station (with lower Linear Priority number) grabbed the link and will withhold itself from transmission.

Exponential Priority

This number provides priority by affecting the average Exponential Backoff delay.

If:

EP - is the exponential priority number.

N - is the number of collisions.

r - is random number multiplicant of the Slot Time.

Then, r is chosen randomly according to the following:

$0 \le r < 2^{(N+EP, 10)}$

Thus, for EP = 0, we simply get the Ethernet Exponential Backoff Delay.

Exponential Backoff Method

Determines when to start the backoff timeout:

0 - According to the 3-company standard, immediatley after the jamming, concurrently with Interpacket spacing.

1 - After the deferring period expires. This method prevents inefficiency and throughput loss at short topologies and low bit rates where Interpacket Spacing may be longer than the Slot Time.

Interframe Spacing

Specifies the time period, in TxC units, that the 82586 must wait after detecting loss of Carrier Sense before it can begin transmission or reception of a packet. The minimum value is 32 and any value less than that will default to 32. However, during DUMP STATUS command execution, the original configuration number will be read out.

Slot Time

The network Slot Time number or number of TxC cycles in the Slot Time. This value is the basis for backoff delay generation. Zero Slot Time number will be interpreted by the 82586 as 2048.

Promiscuous Mode

If configured to Promiscuous Mode, the 82586 will accept packets independently of the Destination Address.

Broadcast Disable

Disables reception of packets with Broadcast Address even via the Multicast mechanism. Promiscuous Mode bit overwrites the Broadcast Disable Mode.

Manchester/NRZ

Specifies whether NRZ or Manchester encoding/decoding is to be performed.

0 - NRZ.

1 - Manchester.

Note, in Manchester mode there is a need for external receive clock recovery logic from the receive data.

Transmit on No CRS

If set, allows transmission even if there is no CRS back from the transceiver. Important for transceivers (non-Ethernet) that do not feed back the transmitted signals via the receive pair.

No CRC Insertion

0 - CRC is inserted at the end of the packet.

1 - No CRC insertion - (allows higher level CRC generation).

CRC-16/CRC-32

0 - 32-bit Autodin-II CRC.

1 - 16-bit CCITT CRC.

Bitstuffing/EOC

0 - End of Carrier Framing.

1 - Bitstuffing Framing, with HDLC type start of packet/end of packet delimiters.

Padding

Only valid if Bitstuffing is set. If set to padding mode, the 82586 will append automatically flags to frames, shorter than a Slot Time period. Thus, the activity on the link will be for at least one Slot Time period.

CRS-Filter

Specifies the required minimal width of CRS, in TxC cycle units, before it will be recognized as being Carrier Sense. The Carrier Sense Expired state is recognized immediately.

Internal CRS

Specifies whether Carrier Sense is to be generated internally or externally (via CRS pin).

0 - External.

1 - Internal.

CDT-Filter

Specifies for externally generated Collision Detect the required width of CDT, in TxC cycle units, before Collision Detect will be treated as a collision.

Internal CDT

Specifies whether Collision Detect is to be generated internally or externally (via CDT pin).

0 - External.

1 - Internal.

Operates only with transceivers that do not feed back transmitted data on the receive pair, but can sense some other station data.

Min Packet Length

The minimum packet length in bytes. No packet that is shorter than the minimum will be accepted by the 82586.

NOTE

Apart from this mechanism there are some other limitations on the minimum packet length:

First, packets which are shorter than 6 bytes (even in Save Bad Packet Mode, Promiscuous Mode, Address length of Zero) are discarded. No status is reported on such received packets.

Second, for AC-LOC=0 (when Address Control Location implies data separated from control), also packets shorter than 2 x ADDR-LEN + 2 (not including the Packet Check Sequence) are discarded.

Preamble Length

Selects the length of the preamble including BOF.

00 - 2 bytes.
01 - 4 bytes.
10 - 8 bytes.
11 - 16 bytes.

Number of Retries

The number of retries after collision the 82586 will perform before the transmit attempt is aborted.

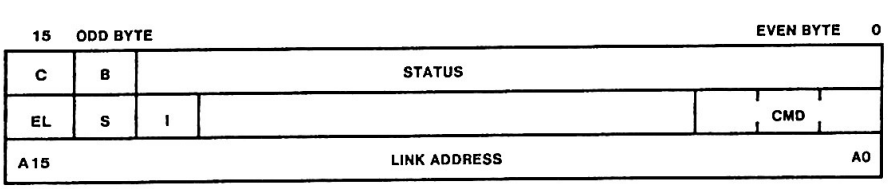
3.2.11.9 Action Commands

The action commands reside in the CBL. The general action command structure is described in Section 3.2.11.3.

a. 82586 Configuration and Set UP.
b. Transmission.
c. Diagnostics oriented.

3.2.11.9.1 NOP

This command results in no action by the 82586 except for that performed in normal command processes. It is present as an aid to CBL manipulation. The format of the NOP command is:



186-032

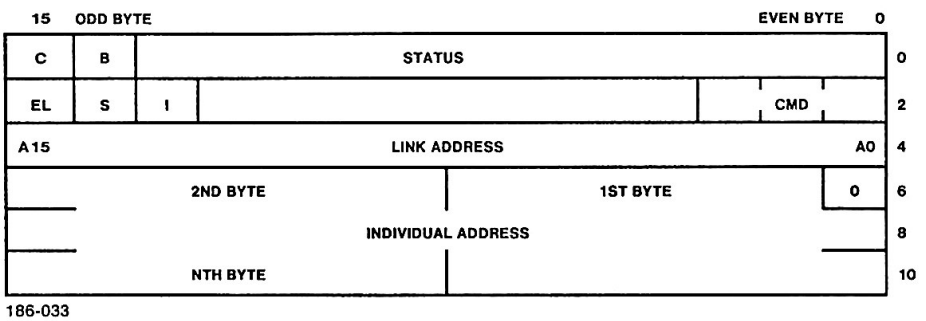
where:

LINK ADDRESS, EL, B, C, I, S	– As per standard CBs
CMD	– The NOP command. Value: 0H.
STATUS	– Bits 12, 13 as per standard CBs

3.2.11.9.2 Individual Address Set-Up

This command is used to load the 82586 with the Individual Address. This address will be used by the 82586 for recognition of Destination Address and insertion of Source Address.

The format is as follows



186-033

where:

LINK ADDRESS, EL, B, C, I, S	– As per standard CBs
CMD	– The ADDRESS SET-UP command. Value: 1H.
STATUS	– Bits 12, 13 as per standard CBs

NOTE

After RESET, prior to Individual Address Setup Command execution, the 82586 assumes the Broadcast Address as the Individual Address in all aspects, i.e:

- o This will be the Individual Address Match reference.
- o This will be the Source Address of a transmitted packet (for AC-LOC=0 mode only).

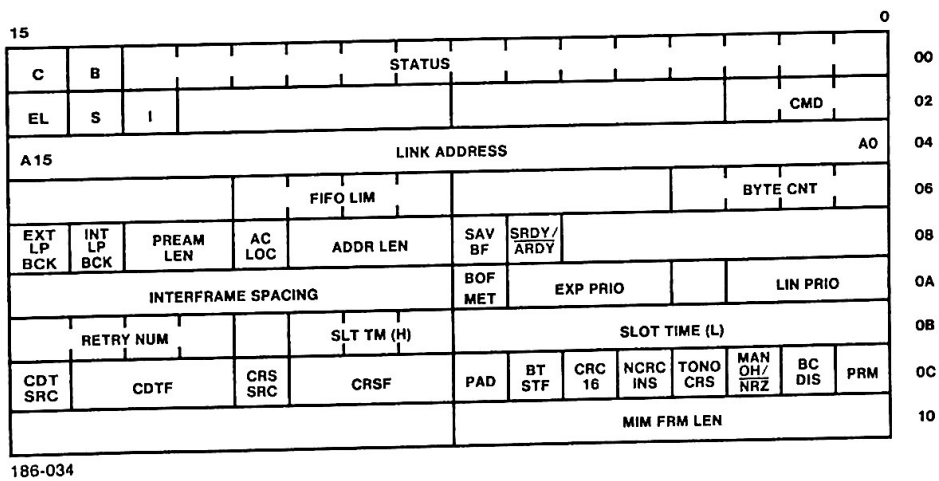
The Individual Address least significant bit must be zero for Ethernet (see the Command Structure). However, no enforcement of 0 is provided by the 82586. Thus, Individual Address with Least Significant Bit 1, is a valid Individual Address in all aspects.

INDIVIDUAL ADDRESS – The individual address of the node.

3.2.11.10 Configure

The Configure Command is used to load the 82586 with its operating parameters. The Configure Command allows changing only part of the parameters by specifying a byte count of less than 12. Any number larger than 12 will be truncated to 12. Any number less than 4 will be rounded to 4.

The format of the Configure command is:



where:

Link Address, EL
B, C, I, S — As in standard CBs

Status — Bits 12, 13 as per standard CBs.

CMD — The configure CMD value: 2H

Byte 1: Byte CNT (Bits 0-3) — Byte count. Number of bytes, including this one, that hold parameters to be changed.

NOTES:
1) In word mode, if programmed to odd number, the last byte is truncated.
2) A number smaller than 4 is interpreted as 4.
3) A number greater than 12 is interpreted as 12.

Byte 2: FIFO LIM (Bits 0-3) — FIFO LIMIT value

Byte 3: SRDY/ARDY (Bit 6)

0 — SRDY/ARDY pin operates as ARDY (internal synchronization).

1 — SRDY/ARY pin operates as SRDY (external synchronization).

SAV BF (Bit 7)

0 — Received bad packets are not saved in the memory.

1 — Received bad packets are saved in the memory.

Byte 4: ADDR LEN – Number of address bytes.
(Bits 0-2)

NOTE: 7 is interpreted as 0.

AC LOC (Bit 3)

0 – Address and Type Fields are separated from data and are associated with Transmit Command Block or Receive Packet Descriptor. For transmitted packet, the Source Address is generated by the 82586.

1 – Address and Type Fields are part of the transmit/receive data buffers, including the Source Address.

PREAM LEN – Preamble Length including Beginning of Packet indicator.
(Bits 4-5)

00 - 2 bytes.
01 - 4 bytes.
10 - 8 bytes.
11 - 16 bytes.

INT LP BCK –Internal Loopback.
(Bit 6)

EXT LP BCK – External Loopback.
(Bit 7)

NOTES: Bits 6 and 7 configured to 1, cause Internal Loopback.

Byte 5: LIN-PRIO – Linear Priority.
(Bits 0-2)
EXP-PRIO – Exponential Priority.
(Bits 4-6)

BOF-MET (Bit 7) – Exponential Backoff Method

0– Ethernet.

1 – Short Topology and/or Low Bit Rate (Intepacket Spacing Shorter than the Slot Time).

Byte 6: INTERFRAME SPACING – Number that indicates the Interpacket Spacing in TxC period units.

NOTES: Number smaller than 32 is interpreted as 32.

Byte 7: SLOT TIME (L) – Slot Time, low byte.

Byte 8: SLT-TM (H) (Bits 0-2) – Slot Time, number, high byte.

NOTES:

1) Slot Time is the Slot Time number of TxC period units.

2) Slot Time Number of zero is interpreted as 2048 (2^{11}).

RETRY-NUM (Bits 4-7) – Number of transmissions retries on collisions.

Byte 9: PRM (Bit 0) – Promiscuous mode

0 - Non Promiscuous address filtering mode.

1 - Promiscuous Mode.

BC-DIS (Bit 1) – Broadcast Disable

0 - Broadcasted packets accepted.

1 - Broadcasted packets rejected.

MANOH/NRZ– Manchester or NRZ encoding/decoding.
(Bit 2)
0 - NRZ
1 - Manchester

TONO CRS – Transmit Or No Carrier Sense
(Bit 3)
0 - Cease transmission if CRS goes inactive during packet transmission (after preamble is sent).
1 - Continue transmission even if there is no Carrier Sense.

NCRC INS – No CRC Insertion
(Bit 4)
0 - 82586 generates and appends FCS to transmitted packets.

CRC 16 – CRC Type
(Bit 5)
0 - 32 bit Autodin II CRC polynomial.
1 - 16 bit CCITT CRC polynomial.

BT STF – Bitstuffing
(Bit 6)
0 - End of Carrier Mode (Ethernet).
1 - HDLC like Bitstuffing mode.

PAD – Padding
(Bit 7)
0 - No padding.
1 - Perform padding by transmitting flags for the rest of the slot time.

NOTE: PAD has meaning only for Bitstuffing. In EOC mode, PAD value is internally enforced to zero.

Byte 10: CRSF (Bits 0-2) – Carrier Sense Filter Bits.

CRS-SRC (Bit 3) – Carrier Sense Source

0 - Carrier Sense Signal externally generated.

1 - Carrier Sense Signal internally generated.

CDTF (Bits 4-6) – Collision Detect Filter Bits.

CDT-SRC (Bit 7) – Collision Detect Source

0 - Collision Detect Signal externally generated.

1 - Collision Detect Signal internally generated.

(Works for a transceiver that does not feed back the transmitted signal on the receive pair).

Byte 11: MIN FRM LEN– Minimum number of bytes in a packet. Packets shorted than the MIN FRM LEN will be treated as bad packets.

Configuration Defaults

The reset configures the 82586 to be compatible with the Ethernet Specifications.

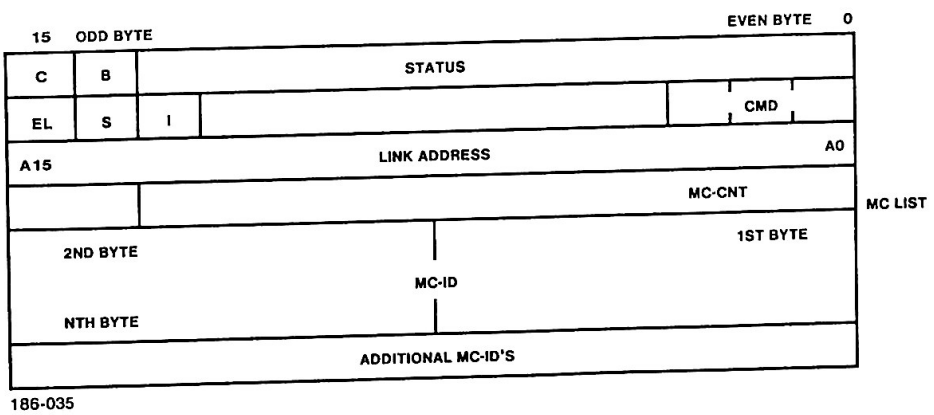
FIFO LIMIT	= 8
SRDY/ARDY	= 0
SAVE BAD FRAME	= 0
ADDRESS LENGTH	= 6
ADDRESS/CONTROL	= 0
FIELD LOCATION	= 0
INT LOOPBACK	= 0
EXT LOOPBACK	= 0
LINEAR PRIORITY	= 0
EXPONENTIAL BACKOFF METHOD	= 0
EXPONENTIAL PRIORITY	= 0
INTERFRAME SPACING	= 96
SLOT TIME	=512

PROMISCUOUS MODE	= 0
BROADCAST DISABLE	= 0
MANCHESTER/NRZ	= 0
TRANSMIT ON NO CRS	= 0
NO CRC INSERTION	= 0
CRC-16/CRC-32	= 0
BITSTUFFING/EOC	= 0
PADDING	= 0
CRS FILTER	= 0
INTERNAL CRS	= 0
INTERNAL CDT	= 0
MIN-FRAME-LENGTH	= 64
PREAMBLE LENGTH	= 2
NUMBER OF RETRIES	= 15

3.2.11.11 Multicast Set-Up Command

This command is used to load the 82586 with the Multicast-IDs that should be accepted. This command resets the current filter and reloads it with the specified Multicast-IDs.

The format of the Multicast Address Set-Up command is:



186-035

where:

LINK ADDRESS, EL,B,C,I,S – As in standard CBs.

STATUS – Bits 12, 13 per standard CB's (see Section 3.2.11.3.1)

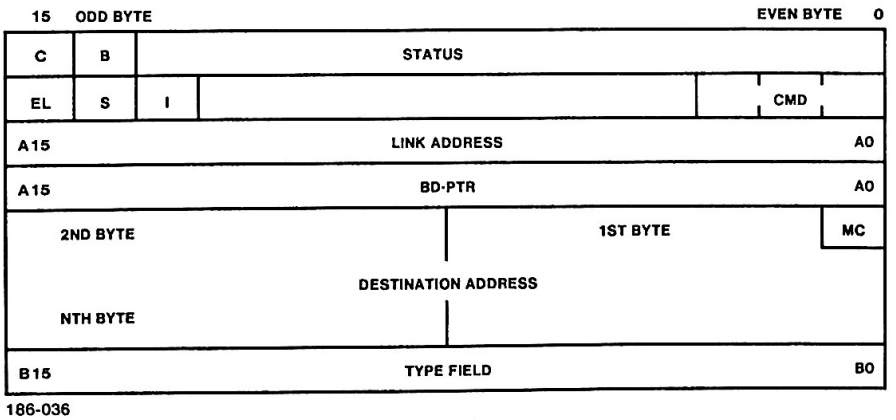
CMD – The MULTICAST ADDRESS SET UP command value: 3H.

MC-CNT – This 14 bit field indicates the number of bytes in the MC LIST field. The MC-CNT used, must be a multiple of the ADDR-LEN, otherwise, the 82586 truncates the MC-CNT to the nearest ADDR-LEN multiple. MC-CNT=0 implies reset of the HASH TABLE which is equivalent to disabling of the Multicast filtering mechanism.

MC LIST – A list of Multicast Addresses to be accepted by the 82586. The least significant bit of each MC address must be "1". Note, the list is compacted, i.e., the most significant byte of the next address is immediately followed by the least significant byte of the next address.

3.2.11.12 Transmit Command

This command is used to transmit a packet of user data onto the serial link. The format of a transmit command is:



186-036

where:

LINK ADDRESS, EL, B,C,I,S – As in standard CBs.

STATUS – Defined bits are:

Bits 12, 13 – As per standard CBs (see Section 3.2.11.3.1).

Bit 10 – No Carrier Sense signal during transmission. Carrier Sense signal is monitored from the end of Preamble transmission until the end of Packet Check Sequence for TONO-CRS =1 (Transmit On No Carrier Sense Mode) it indicates that transmission has been executed despite CRS nonexistence For TONO-CRS=0 (Ethernet) mode, this bit also indicates unsuccessful transmission (transmission stopped when lack of Carrier Sense has been detected).

Bit 9 – Transmission unsuccessful (stopped) due to Loss of Clear to Send signal.

Bit 8 – Transmission unsuccessful (stopped) due to DMA Underrun, i.e., data not supplied from the system for transmission.

Bit 7 – Transmission Deferred, i.e. transmission was not immediate due to 82586 deferring transmission as a result of previous link activity.

Bit 6 – Heart Beat Indicates, that after previously performed transmission, and before the recently performed transmission, (Interpacket Spacing) CDT signal was monitored being active. This indicates that the Ethernet Transceiver Collision Detect Logic performs well.

The Heartbeat is monitored during the Interpacket Spacing Period.

Bit 5 – Transmission attempt stopped due Too Many Collisions. This happens if the number of retries is exhausted.

Bits 3-0 – Number of Collisions experienced by recently transmitted packet.

CMD – TheTRANSMIT command: 4H

BD-PTR – The offset portion of the address of the first TBD containing transmit data. BD-PTR=OFFFFH indicates no TBD is used.

Destination Address – Contains the Destination Address for the packet. The least significant bit (MC) indicates the address type:
MC = 0: Individual Address.
MC = 1: Multicast or Broadcast Addresses.
If the destination Address bits are All Ones this is a Broadcast Address.

Type Field – The contents of this field are user defined.

NOTE:

1. The DESTINATION ADDRESS and the TYPE FIELD are packed i.e. the TYPE-FIELD's least significant byte follows immediately the DESTINATION ADDRESS's most significant byte.

2. The DESTINATION ADDRESS and TYPE FIELD are not used when the 82586 is configured to AC-LOC=0.

3. For AC-LOC=1 transmit buffers shorted than ADDR-LEN are invalid. The transmission will be aborted by DMA Underrun.

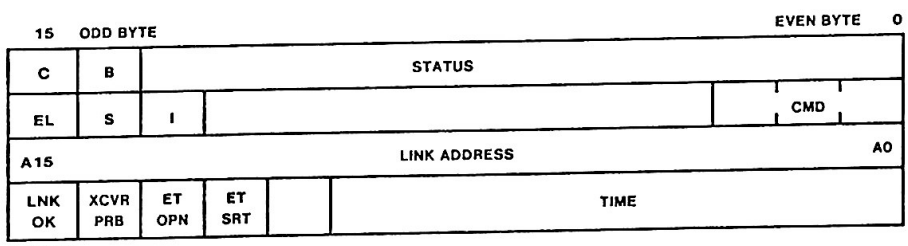
4. Packets which are aborted in the middle of transmission (can result from any reason indicated by any of the STATUS bits 8, 9, 10, and 12) are jammed.

5. Jamming Rules:
   a. Jamming will not start before completion of preamble transmission.
   b. Collision detected during transmission of the last 11 bits will not result in jamming.

   If the collision is detected during the transmission of the last bit or later, the collision will not be reported and retransmission will not take place. This may happen for invalid packet which is shorter in length than the Slot Time.

3.2.11.13 TDR

This command performs a Time Domain Reflectometer test on the serial line. By performing the command, the user is able to identify shorts or opens and their location on the network. Along with transmission of All Ones, the 82586 triggers an internal timer. The timer measures the time elapsed from transmission start until "echo" is obtained. "Echo" is indicated by Collision Detect going active or Carrier Sense signal drop.



186-037

where:

Link Address, EL, B,C,I,S – As in standard CBs.

STATUS – Bits 12, 13 per standard CBs (see Section 3.2.11.3.1).

CMD – The TDR command value: 5H.

TIME – An 11-bit field that specifies the number of TxC cycles that elapsed before "echo" was observed. All Ones indicates no echo.

NOTE, due to the network consisting of various elements as transceiver links, transceivers, Ethernet, repeaters, etc, the TIME is not exactly proportional to problem distance.

The accuracy of problem location is 0.5 Vs/fs where:
Vs - the wave propogation speed on the link.
fs - the serial clock frequency.

LNK OK (Bit 15) – No link problem identifed. TIME - 7FF H.

XCVR PRB (Bit 14) – Transceiver Link Problem identified. LNK-OK=O. TIME-7FFH.

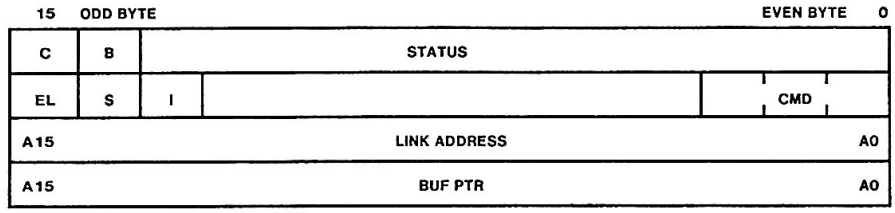
ET OPN (Bit 13) – Open on the Ethernet link identified LNK-OK=0.

ET SRT (Bit 12) – Short on the Ethernet link identified. LNK-OK=0.

3.2.11.14 DUMP STATUS

This command causes the contents of various 82586 registers to be placed in memory. It is supplied as an 82586 self diagnostic means plus access to registers of interest to the user.

The DUMP STATUS command format is:



186-038

where:

Link Address, EL, B,C,I,S – As in standard CBs (see Section 3.2.11.3.1).

CMD – The DIAGNOSE command value: 6H.

STATUS – Bits 12, 13 per standard CBs (see Section 3.2.11.3.1).

BUF PTR – This 16-bit quantity specifies the offset portion of the memory address which points to the top of the buffer allocated for the dumper registers content.

NOTE: The user of the DUMP STATUS command, must allocate a 170 byte buffer for this purpose.

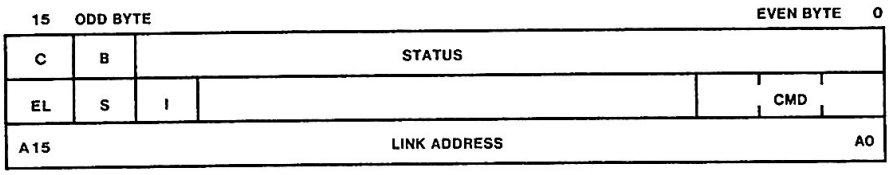
3.2.11.15 Diagnose

The Diagnose Command checks the internal to the 82586 timer hardware which includes:

- o Exponential Backoff Random Number Generator (Free Run Counter).
- o Exponential Backoff Timeout Counter.
- o Slot Time Period Counter.
- o Collision Number Counter.
- o Exponential Backoff Shift Register.

- o Exponential Backoff Mask Logic.
- o Timer Trigger Logic.

The DIAGNOSE Command Format is:



186-039

where:

Link Address, EL, B,C,I,S – As in standard CBs (see Section 3.2.11.3.1)

STATUS – Bits 12, 13 per standard CBs (see Section 3.2.1.3.1)

CMD – The DIAGNOSE command value: 7H.

The DIAGNOSE is performed in two phases.

3.2.11.15.1 (Counters Test), Phase 1

The Free Run, Exponential Backoff Timeout, Slot Time and Collision Counters are checked. Misinterpretation of stuck in state counter as a positive result is avoided by checking the counters when peforming transition.

The test is performed in the following steps:

a. All counters are RESET at once.
b. Count.

c. Stop counting when the Free Run counter (10 bits), Exponential Backoff Counter (10 bits), wrap from All Ones to All Zeros. Simultaneously Slot Time counter switches from 01111111111 to 10000000000 and the collision counter (4 bits) wraps from All Ones to All Zeros.

Note: Counting is stopped if any of the 3 longer counters wrap, as described above.

d. The 10 least significant bits (if they exist) are checked for being All Zeros.

If the PHASE 1 passes successfully, this means all the counters count properly, including the Free Run Counter.

3.2.11.15.2 (Trigger Logic Test), Phase 2

a. Reset the Exponential Backoff Shift Register, and all the counters.
b. Configure internally the Exponential Backoff logic according to the following:

SLOT TIME	= 8H
LIN-PRIO	= 2H
EXP-PRIO	= 1H
BOF-MET	= 0H

c. Emulate internally transmission and collision.
d. Is the most significant bit of Exponential Backoff Shift Register 1? If not, go to Step c. If yes, continue.
e. Check the Mask Logic Output for being All Ones (the Free Run Counter is All Ones at this point and the Exponential Backoff Shift Register is also All Ones).

If Step e's result is positive, "passed" status is issued; otherwise, "failed" status is issued.

3.2.12 LOCAL MEMORY PROGRAMMING

The local memory consists of six 28-pin JEDEC sites and 16K Bytes of iRMX 86 Kernel memory in the 80130A device. The sites are configured as pairs to create a 16-bit data bus. The 16K Bytes of 80130A kernel memory is considered as a site pair. Table 3-14 shows the address ranges for the site pairs based on the socket size selected.

NOTE

When using 4K memory devices the iRMX Kernel code (80130A Kernel) cannot be accessed.

Table 3-14. Local Memory JEDEC Site Address Ranges

ODD ADR (Upper)	EVEN ADR (Lower)	4K Devices	8K Devices (Hex)	16K Devices (Hex)	32K Devices (Hex)
80186 ADDRESSES					
U34	U51	FE000-FFFFF	FC000-FFFFF	F8000-FFFFF	F0000-FFFFF
80130A Kernel		See Note	F8000-FBFFF	F0000-F7FFF	E0000-EFFFF
U33	U50	FA000-FBFFF	F4000-F7FFF	E8000-EFFFF	D0000-DFFFF
U32	U49	FB000-F9FFF	F0000-F3FFF	E0000-E7FFF	C0000-CFFFF
82586 ADDRESSES*					
U34	U51	0FE000-0FFFFF	0FC000-0FFFFF	0F8000-0FFFFF	0F0000-0FFFF
80130A Kernel		See Note	0F8000-0FBFFF	0F0000-0F7FFF	0E0000-0EFFFF
U33	U50	0FA000-0FBFFF	0F4000-0F7FFF	0F8000-0EFFFF	0D0000-0DFFFF
U32	U49	0FB000-0F9FFF	0F0000-0F3FFF	0E0000-0E7FFF	0C0000-0CFFFF

NOTE: If memory devices of 4K capacity or less are installed, the 80130A's iRMX kernel cannot be used. However, the timer and interrupt controller features of the 80130A device can be used with 4K memory devices.
* Shown with leading 0's to indicate 24-bit address.

3.2.13 LOCAL I/O PROGRAMMING

Programming for the following local I/O are discussed in paragraphs 3.2.14 through 3.4.

- Serial I/O Programming.
- Parallel I/O Programming.

- o Timers and DMA Programming.
- o Interrupt Control Programming.
- o iSBX Interfaces Programming.

Table 3-15 lists the local I/O port assignments. I/O addresses 0080(H) to 00FF(H) are always assumed to be on the iSBC 186/51S board. The peripheral control block resides at addresses FF00(H) to FFFF(H). All other addresses are assumed to be on the MULTIBUS system.

Table 3-15. Local I/O Port Address Assignments

Address	Device Selected	Function
0080-008E (Even)	iSBX 1 (J5)	Byte Access: 8- or 16-bit, iSBX Bus, SBX1CS0/ active. Word Access: 16-bit, iSBX Bus, SBX1CS0/ and SBX1CS1/ active.
0081-008F (Odd)	iSBX 1 (J5)	Byte Access: 16-bit, iSBX Bus, SBX1CS1/ active. Word Access: Not Applicable.
0090-009E (Even)	iSBX 1 (J5)	Byte Access: 8-bit, iSBX Bus, SBX1CS1/ active.
00A0-00AE (Even)	iSBX 2 (J4)	Byte Access: 8- or 16-bit, iSBX Bus, SBX2CS0/ active. Word Access: 16-bit, iSBX Bus, SBX2CS0/ and SBX2CS1/ active.
00A1-00AF (Odd)	iSBX 2 (J4)	Byte Access: 16-bit, iSBX Bus, SBX2CS1/ active. Word Access: Not Applicable.
00B0-00BE (Even)	iSBX 2 (J4)	Byte Access: 8-bit, iSBX Bus, SBX2CS1/ active. Word Access: Not Applicable.
00C8	82586	82586 Wakeup: Byte or word, data insignificant.

Table 3-15. Local I/O Port Address Assignments (Cont'd.)

Address	Device Selected	Function
OOCB	Programmable Latch (U26) (74LS259)	Byte Access: Write Only. Word Access: Not Applicable.
OOD0	16M Byte Window Latch, (U73) (8283)	Byte Access: Write Only. Word Access: Not Applicable.
OOD2	Flag Byte Signalling PAL U83	Byte Access: Write Only. Word Access: Not Applicable.
OOCC	Configuration Input U35	Byte Access: Read Only. Word Access: Not Applicable.
OOCE	Reset Latched Inputs	Byte Access: Data insignificant. Word Access: Data insignificant.
OOD4	iSBX1 (J5)	Byte Access: 8-bit, iSBX Bus, MDACK1/ active. Word Access: 16-bit, iSBX Bus, MDACK1/ active.
OOD6	iSBX2 (J4)	Byte Access: 8-bit, iSBX Bus, MDACK2/ active. Word Access: 16-bit, iSBX Bus, MDACK2/ active.
OOD8	8274 (U2)	Byte Access: Channel A Data. Word Access: Not Applicable.
00DA	8274 (U2)	Byte Access: Channel B Data. Word Access: Not Applicable
OODC	8274 (U2)	Byte Access: Channel A Control/Status. Word Access: Not Applicable.
OODE	8274 (U2)	Byte Access: Channel B Control/Status. Word Access: Not Applicable.

Table 3-15. Local I/O Port Address Assignments (Cont'd.)

Address	Device Selected	Function
OOE0-00E2	80130A (U16)	Byte Access Only: Interrupt Controller.
00E8	80130A (U16)	Byte Access Only - Systick Timer.
00EA	80130A (U16)	Byte Access Only - Delay Counter.
OOEC	80130A (U16)	Byte Access Only - Baud Rate Timer.
00EE	80130A (U16)	Byte Access Only - Timer Control.
OOFO	Ethernet Station Address	Most Significant Byte. Byte Access: Read Only. Word Access: Not Applicable.
OOF2	Ethernet Station Address	Second Most Significant Byte. Byte Access: Read Only. Word Access: Not Applicable.
OOF4	Ethernet Station Address	Third Most Significant Byte. Byte Access: Read Only. Word Access: Not Applicable.
OOF6	Ethernet Station Address	Fourth Most Significant Byte. Byte Access: Read Only. Word Access: Not Applicable.
OOF8	Ethernet Station Address	Fifth Most Significant Byte. Byte Access: Read Only. Word Access: Not Applicable.
OOFA	Ethernet Station Address	Least Significant Byte. Byte Access: Read Only. Word Access: Not Applicable.

3.2.14 SERIAL I/O PROGRAMMING

The iSBC 186/51S board supports all modes of the 8274 Multi-protocol Serial Controller (MPSC) except external sync detect. For direct-vectored interrupt operation, the 8274 Controller is programmed for 8086 vectored mode operation and a base vector must be supplied. Detailed programming instructions for the 8274 Controller is provided in the 8274 Multi-protocol Serial Controller Data Sheet in the Intel Component Data Catalog. The document is available from the:

Intel Corporation
Literature Department SV3-3
3065 Bowers Avenue
Santa Clara, CA 95051

Baud rate programming for the 80130A and 80186 timers are available in Tables 3-16 and 3-17. "How to" instructions for programming the 80130A timers are shown in Table 3-18. Instructions for programming the 80186 timers are shown in Section 3.2.8.

Table 3-16. 8274 MPSC Asynchronous Baud Rate Programming

Baud	Timer	
	80130A	80186
19200	19	----
9600	39	----
4800	78	19
2400	156	39
1200	312	78
600	625	156
300	1250	312

Table 3-17. 8274 MPSC Synchronous Baud Rate Programming

Baud	Timer	
	80130A	80186
125000	48	12
64000	93	24
48000	126	32
19200	312	78
9600	625	156

3.2.15 80130A TIMER PROGRAMMING

The following paragraphs describe 80130A timer programming.

3.2.15.1 Programmable Timers

The 80130A contains three programmable timers. Each timer has 16-bit resolution. The functions of each timer are restricted to a fixed mode of operation needed by the RMX nucleus. The function are as follows:

Timer O: Operating Clock Reference – This timer is used to set a given time reference for nucleus interrupts. The input clock to this timer is the CLK chip input. The output is connected to the System Clock Tick output pin (SYSTICK), as well as internally to the input clock of Timer 1.

Timer 1: Programmable Delay Timer – This timer is used to time out the shortest delay the nucleus is aware of. The input clock to this timer is derived from the output of timer 0. The output is connected to stake pin E79.

Timer 2: Baud Rate Generator – This timer is used to generate the baud reference use in serial communication of the system. The input clock is the chip CLK input and the output is connected to the BAUD output pin.

The Timers are connected to the lower half of the data bus and hence are addressed as even addresses. The timers registers are located at the following I/O addresses and are accessed by IOCS=0 and the appropriate peripheral read/write cycle:

Timer 0	8H
Timer 1	0AH
Timer 2	OCH
Timer Control	OEH

The Timer Control register allows the latching of the count of timer 0, 1 or 2 so their content may be read without interfering with counter operation.

In reading/writing the timers, the least significant byte is always accessed first, then the most significant byte. It is not possible to read/write any one entire timer contents in a single 16-bit operation.

3.2.15.2 Timer Control

The 80186 processor controls the operational mode of each timer. The 80130A restricts the programmability of each timer so that the control word is a single fixed byte value to initialize the corresponding timer. The formats accepted by the 80130A for mode definition of each timer is as follows:

Timer 0. Initialization Word

0	0	1	1	1	0	1	0	-	Command Word (80130A recognizes 001XXXXX).
0	0	-	-	-	-	-	-	-	Select Timer 0.
-	-	1	1	-	-	-	-	-	Least Significant Bytes, then Most Significant Bytes.
-	-	-	-	0	1	0	-	-	Mode 2 (Rate Generator).
-	-	-	-	-	-	-	0	-	Binary Counter Mode.

Timer 1. Initialization Word

0	1	1	1	0	0	0	0	-	Command Word (80130A recognizes 011XXXXX).
0	1	-	-	-	-	-	-	-	Select Timer 1.
-	-	1	1	-	-	-	-	-	Least Significant Bytes, then Most Significant Bytes.
-	-	-	-	0	0	0	-	-	Mode 0 (Interrupt on Count).
-	-	-	-	-	-	-	0	-	Binary Counter Mode.

Timer 2. Initialization Word

1 0 1 1 0 1 1 0 -	Command Word (80130A recognizes 101XXXXX).
1 0 - - - - - - -	Select Timer 2.
- - 1 1 - - - - -	Least Significant Bytes, then Most Significant Bytes.
- - - - 0 1 1 - -	Mode 3 (Square Wave Generator).
- - - - - - - 0 -	Binary Counter Mode.

3.2.15.3 Counter Latching Command

The counter latching command is a software command. It freezes the current value of the timer it commands. The values which are allowed and written to I/O address EEH are:

0 0 0 0 0 0 0 0 -	Latch count in Timer 0. (80130A recognizes 000XXXXX).
0 1 0 0 0 0 0 0 -	Latch count in Timer 1. (80130A recognizes 010XXXXX).
1 0 0 0 0 0 0 0 -	Latch count in Timer 2. (80130A recognizes 100XXXXX).

3.2.15.4 Description of Timer Modes

Each timer can be thought of as consisting of three elements:

1. A count register (CR).
2. A counting element (CE).
3. An output latch (OI) (Only for timers 0 and 1).

The count register (CR) is loaded from the data bus upon the appropriate write cycles and contains the initial value to be used by the counting element (CE) when a counting sequence is initiated. The CR can be changed while counting is in progress; the effect of writing into the CR while counting is different for the different modes of operation and is explained later.

The output latch (OL) allows for the storing of the contents of the CE for subsequent program interrogation. Storing the CE in the OL simply saves the current value of the CE in the OL; this has no effect on the counting operation currently in progress.

Unless specifically directed by a latch command, the OL follows the CE value. A latch command freezes the contents of the OL. Reading the OL implicitly unlatches the OL, and it once again tracks the CE.

3.2.15.5 Timer 0 Operation

Timer 0 is pre-defined to operate in Rate Generator mode (Mode 2). In this mode, the output SYSTICK, will initially be high until the CR is loaded. The first falling edge of the clock after the CR is loaded causes the CR to be transferred to the CE. Subsequent falling edges of the clock cause the CE to count. The output goes low for the clock cycle when CE is equal to 1 and is high for other CE values. The next clock automatically reloads the CE from the CR, and subsequent clocks count.

If the CR is loaded during counting and prior to the time that the CR is automatically transferred to the CE (ie., at the clock where the CE would normally decrement from 1 to 0), then the new value in the CR will be transferred to the CE at that time. If only one of two bytes is loaded by the time the automatic transfer of the CR to the CE takes place, then the old value is used. In no case does loading the CR effect any count in progress.

Loading the CR with 0 is a special case. As previously mentioned, the first clock transfers the CR to the CE , and subsequent clocks count. The output pulses low when the CE decrements to 0; thus, the output will pulse every 10000H clocks after the CR is loaded with 0.

Loading the CR with 1 is another special case. The first clock transfers the CR to CE and since 1 is the terminating value, the next clock automatically reloads the CE from the CR. Therefore, if the CR value is still the output, SYSTICK will remain low.

3.2.15.6 Timer 1 Operation

Timer 1 is pre-defined to operate in the Interrupt on Terminal Count mode (Mode 0). The output, DELAY, initially is low and remains low until the CR is loaded. The first falling edge of the clock after the CR is loaded cuases the CR to be transferred to the CE. Subsequent falling edges of the clock cause the CE to down count to 0. The output goes high when the content of the CE is 0. The CE continues to count thereafter.

If a new value is loaded in the CR prior to the expiration of the count, the old count is aborted and the first falling edge of the clock after the CR is loaded causes the CR to be transferred to the CE, and subsequent clocks count. The CE is frozen and the output remains low during the time after the first byte is written and before the second byte is written.

Loading the CR with 0 is a special case. As previously mentioned, the first clock transfers the CR to the CE, and subsequent clocks count. The output goes high when the CE decrements to 0; thus output will go high FFFFH + 2 clocks after the CR is loaded with 0.

3.2.15.7 Timer 2 Operation

The output, BAUD, is initially high and remains high until the CR is loaded. The first falling edge of the clock after the CR is loaded causes the CR to be transferred to CE. Subsequent falling edges of the clock cause the CE to count. The output stays high for N/2 ((N-1)/2 if N is odd) counts and then goes low for N/2 ((N-1)/2 if N is odd) counts. On the falling edge of the clock which signifies the final count for the output in the low state, the output returns to the high state and the CR is automatically transferred to the CE. Then the whole process is repeated. Subsequent falling edges of the clock count N/2 or (N+1)/2 counts while the output is high, then the output goes low for N/2 or N-1)/2 counts, and so on.

Loading the CR while counting works as in timer 0. If the CR is loaded at the time the CR is automatically transferred to the CE, then the new value is used; otherwise the old value is used.

Loading the CR with 0 causes the output to be high for (FFFFH +1) divided by 2 counts, then low for (FFFFH+1) divided by 2 counts.

Loading the CR with 1 causes the output to be high for (FFFFH + 1) divided by 2+1 counts, then low for (FFFFH+1) divided by 2 counts.

All CR values that are not 0 or 1 will count as previously described.

Tables 3-16 and 3-17 (page 3-104) show the Baud Rates using Counter 2 (80130A Timer) for both asynchronous and synchronous operation.

3.2.15.8 Timer Read Operation

Reading a timer value always is least significant byte first and then the most significant byte. The 80130A automatically latches the count of a timer into the OL whenever the LSB is read unless an earlier latch command was issued for that timer. This insures the MSB is the true extension of the LSB. A latch command transfers the current count for the address timer into its output latch (OL). Reading the MSB unlatches the value for the next operation. If a timer is latched and then, some time later, latched again before it was read, the second latch command is ignored.

3.2.16 PARALLEL I/O PROGRAMMING

Programmable latch U26 is used to create eight parallel output bits which are dedicated for on-board functions. Four parallel inputs are also available for soft configuration or dedicated on-board functions. The functions of the programmable latch output lines are shown in Table 3-18 along with the input states that cause them.

3.2.17 DMA PROGRAMMING

There are two DMA channels integrated into the 80186 processor and default wired to the 8274 MPSC serial Channel A. The two channels can be used with the iSBX interfaces by installing push-on jumpers (E70 to E72 and E24 to E21). Although the DMA channels can be used for memory-to-memory transfers, such as moving data from the MULTIBUS to on-board memory, this operation is not recommended.

A string move is just as fast. Also, string moves have a lower priority than DMA, so interrupts can be recognized. Programming for the 80186 DMA channels is shown in Section 3.2.7.

Table 3-18. Programmable Latch U26 Inputs and Outputs

Inputs B	A	9	8	Outputs/Functions
0	0	0	0	Q0 low, loopback Ethernet Channel at ESI
0	0	0	1	Q1 low, not used
0	0	1	0	Q2 low, disable nonmaskable interrupts
0	0	1	1	Q3 low, disable MULTIBUS locked override
0	1	0	0	Q4 high, disable non-volatile RAMs
0	1	0	1	Q5 low, turn off MULTIBUS interrupt
0	1	1	0	Q6 low, turn off diagnostic LED DS3
0	1	1	1	Q7 low, turn off diagnostic LED DS4
1	0	0	0	Q0 high, disable loopback Ethernet Channel at ESI
1	0	0	1	Q1 high, not used
1	0	1	0	Q2 high, enable nonmaskable interrupts.
1	0	1	1	Q3 high, enable MULTIBUS locked override
1	1	0	0	Q4 low, enable non-volatile RAMs
1	1	0	1	Q5 high, turn on MULTIBUS interrupt
1	1	1	0	Q6 high, turn on diagnostic LED DS3
1	1	1	1	Q7 high, turn on diagnostic LED DS2.

The assignments of the four parallel lines are shown in Table 3-19.

Table 3-19. Parallel Input Line Assignments

Jumper	Data Bit Read	Function
E129 to E126	Bit 3	Unassigned (user designated)
E123 to E122	Bit 2	Unassigned (user designated)
E128 to E124	Bit 1	Unassigned (user designated)
E133 to E134	Bit 0	Unassigned (user designated)

3.2.18 INTERRUPT CONTROL

The iSBC 186/51S board includes an 80130A device which incorporates an interrupt controller in addition to the interrupt controller built into the 80186 processor. The

80130A controller is the master controller, the 80186 controller is the slave controller. The 80130A controller must be programmed to indicate which interrupt level the 80186 slave controller is connected to. In the as shipped (default) configuration, the 80186 microprocessor is connected to IR4 and the 8274 Multi-Protocol Serial Control is connected to IR3. If the 8274 is not connected to IR3 but is to be used, PAL U30 must be reprogrammed. Section 3.2.10 shows the 80130A PIC programming.

3.3 iSBX™ Interfaces

The iSBX interfaces can be accessed in a byte mode or word depending on the iSBX multimodule installed. Refer to the hardware reference manual for the installed multimodules, for programming instructions.

3.4 Flag Byte Signalling

The iSBC 186/51S board uses a method called flag byte for interrupt level signalling between the on-board 80186 processor and a MULTIBUS processor. A MULTIBUS I/O address is selected by means of jumpers on the board. Data written to that address determines what action is taken. MULTIBUS I/O address selection is shown in Table 3-20 for both 8- and 16-bit data transfer configurations. Flag byte signalling codes are shown in Table 3-21.

Table 3-20. MULTIBUS® I/O Address Selection

Jumpers Installed			Address Selected	
E210 to E206	E211 to E207	E212 to E208	16 Bit Transfer E213 to E209	8 Bit Transfer E209 to E205
X	X	X	08A4	A4
X	X	-	08A5	A5
X	-	X	08A6	A6
X	-	-	08A7	A7
-	X	X	09A4	A4
-	X	-	09A5	A5
-	-	X	09A6	A6
-	-	-	09A7	A7

NOTE: X = Jumper Installed
- = Jumper Removed

Table 3-21. Flag Byte Signalling Codes

Data Written	Data Written To		Action
	iSBC 186/51S	MULTIBUS	
04	X		Clear Interrupt to the iSBC 186/51S board
04		X	Clear Interrupt to MULTIBUS processor
02	X		Set Interrupt to MULTIBUS processor
02		X	Set Interrupt to iSBC 186/51S board
01	X		Clear Interrupt to MULTIBUS processor
01		X	Reset iSBC 186/51S board

NOTE: All other codes are illegal. Reading the port from either side will yield indeterminate results.

CHAPTER 4. PRINCIPLES OF OPERATION

4.1 Introduction

This section provides the principles of operation for the iSBC 186/51S board. The discussion is presented under three major headings; Functional Description, Circuit Descriptions and Operations. The functional description defines and describes the major functional blocks of the board. The circuit descriptions describe in detail the operation of the functional blocks defined in the "Functional Description". The Operation section describes the operating cycles of the board.

4.2 Functional Description

Figure 4-1 is a block diagram of the iSBC 186/51S board. It shows the major functional elements of the board. The following paragraphs discuss the major circuit elements. Detailed circuit descriptions for the more complex circuit blocks are provided in paragraph 4.2.1 through 4.2.14.

4.2.1 iSBC® 186/51S BOARD CLOCKS

There are five clock signals on the iSBC 186/51S board. They are shown in Figure 4-2 and listed below:

1. The 12MHz Clock (16M CLK),
2. The 6MHz Processor Clock (CLK and BUFF CLK),
3. The 3MHz Processor Clock (PCLK),
4. The 10MHz Ethernet Clock (TXC), and
5. A 25MHz Clock for the Dynamic RAM Controller.

The 12MHz clock (16M CLK) is generated by DIP crystal oscillator G1. This clock is used by the Dual Port Arbitration Logic and is also the master clock input to the 80186 processor.

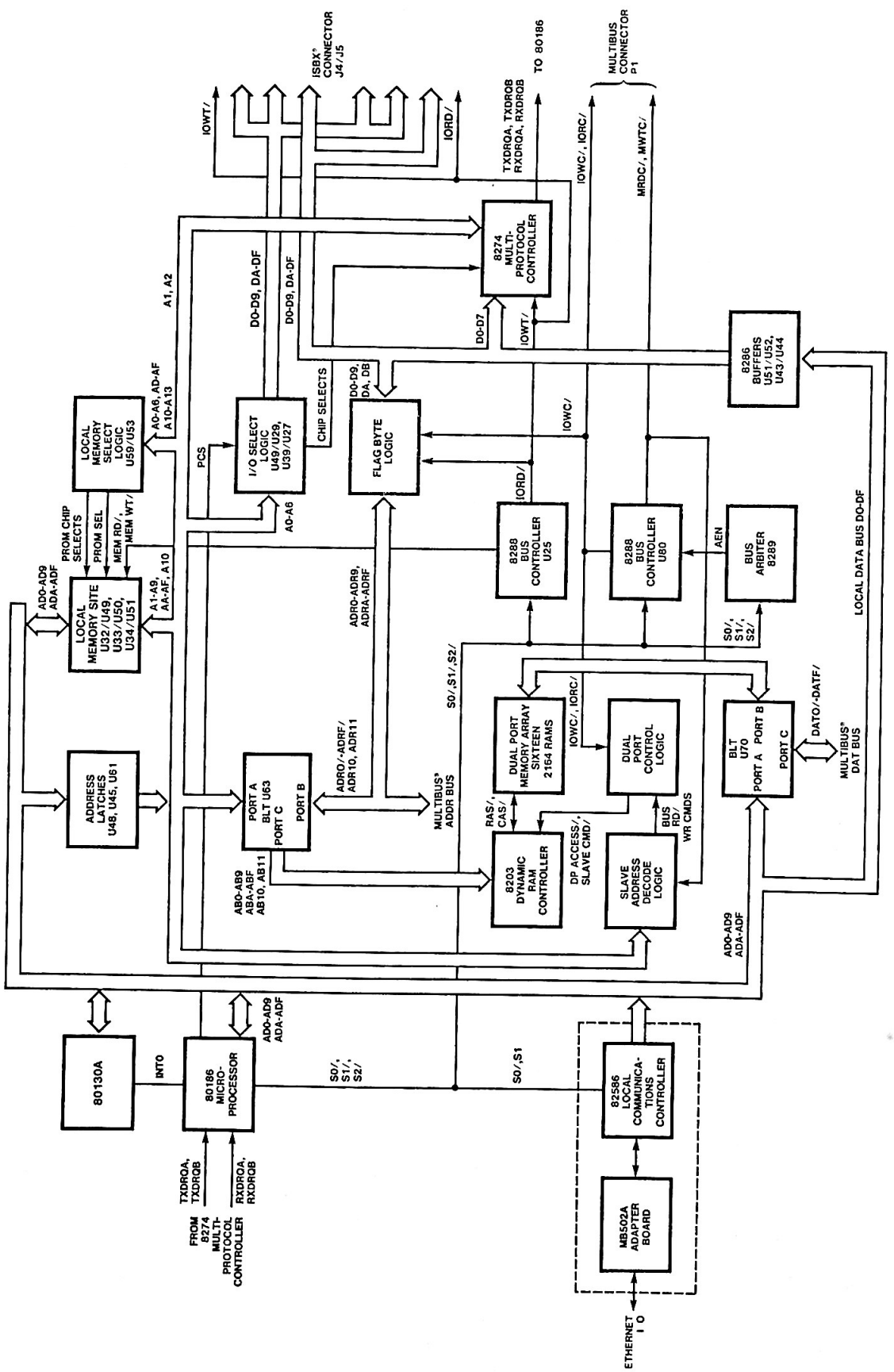


Figure 4-1. iSBC® 186/51S COMMputer™ Block Diagram

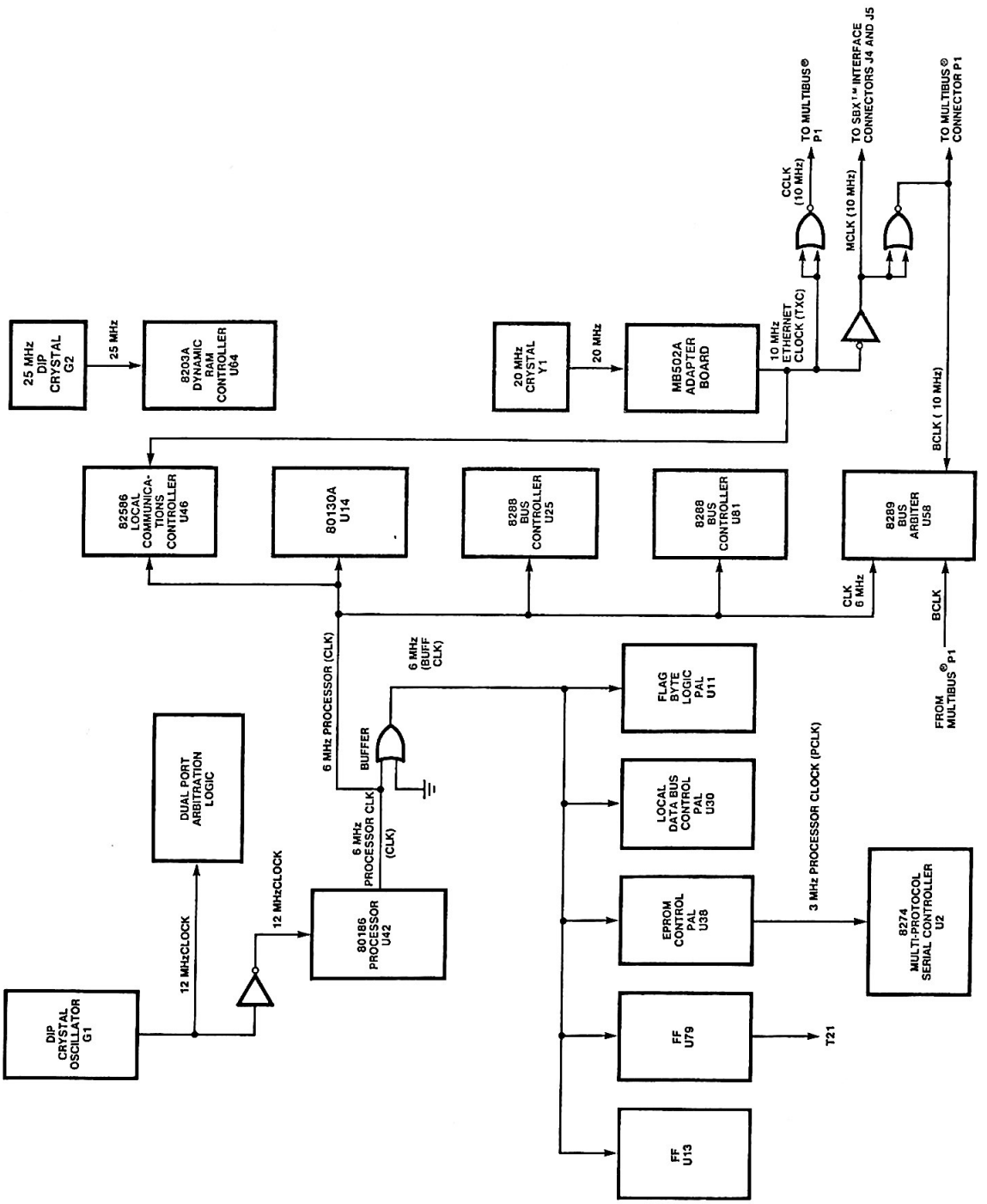


Figure 4-2. iSBC® 186/51S Board Clocks

The 6MHz Processor Clock (CLK) is derived in the 80186 Processor from the 12MHz Clock. CLK is tied directly to the 82586 Local Communication Controller, the 80130A, the two 8288 Bus Controllers and the 8289 Bus Arbiter. CLK is buffered and becomes BUFF CLK which is applied to EPROM Control PAL U38, Local Data Bus Control PAL U30, Flag Byte Logic PAL U11, T21 flip-flop U79 and timeout flip-flop U13.

The 3MHz Processor Clock (PCLK) is derived in EPROM Control PAL U38 from BUFF CLK. PCLK is the clock input to the 8274 Multi-Protocol Serial Controller U2.

The 10MHz clock is derived from the 20MHz crystal on the MB 502A Adapter Board. It exits the MB502A as the Ethernet Transmit Clock (TXC), and is applied directly to the 82586 chip located at U46. TXC is also buffered and becomes MULTIBUS clocks BCLK (Bus Clock), CCLK (Constant Clock), and MCLK (MULTIBUS Clock).

NOTE

The MB502A Adapter Board connects to the iSBC 186/51S Board through the connector at U31.

A 25MHz crystal oscillator at G2 supplies the interval timing clock for the 8203 Dynamic RAM Controller at U64.

4.2.2 80186 MICROPROCESSOR

The main processor on the iSBC 186/51S board is an Intel 80186 16-bit Microprocessor. The 80186 is software compatible with the Intel 8086. The 80186 device is a highly integrated processor and includes a CPU, a bus controller, ready logic, chip select logic, clock generator, reset logic, timers, DMA controllers and interrupt controller. Not all of the 80186 functions are used on the iSBC 186/51S.

The 80186 CPU function is used on the board.

The internal bus controller of the 80186 is not used, since the 80186 is in the MAX mode.

The asynchronous ready logic is used on the 80186 as it is on the 82586. The 80186 is programmed for Upper Memory Chip Select (UCS) and Middle Memory Chip Select (MCS) with zero wait states and external ready required. Peripheral Chip Select (PCS) is programmed for two wait states and external ready required.

The chip select logic in the 80186 is partly used. UCS and LCS are not used at all, however UCS must be programmed as stated above. If the 16 M Byte window onto the MULTIBUS is to be used, then MCS should be programmed for a block size of 256K with a base at MCS0 of 80000(H). This makes the range of MCS0 to MCS3 080000(H) to 0BFFFF(H) which is the address of the 16M Byte window. It is in the MCS0 to MCS3 address range that the WINDOW EN/ signal is active. That signal through a PAL develops WINDOW AEN/ active low. This signal when active enables the 16M Byte Upper Address Latch at U47, which permits the iSBC 186/51S board to access all MULTIBUS memory in the 16M Byte address space.

The DMA Controllers on the 80186 are used (DRQ1, pin 19 and DRQ0 pin 18). Through several sets of stake pin jumpers they can be tied either to the 8274 I/O Serial Controller or to the iSBX bus connectors J4 and J5.

The interrupt controller on the 80186 is used in the RMX mode. It is slaved to the 80130A which acts as the master Programmable Interrupt Controller (PIC).

The PCS (Peripheral Chip Select) is programmed for a base address of 0000(H), and two wait states using external ready. This places all iSBC 186/51S on-board I/O resources at 0080H-00FF(H).

The clock generator on the 80186 is used only in its frequency mode.

The three timers are used. CLKOUT is 6 MHz, derived from the 12 MHz DIP crystal input. TMRIN0 and TIMERIN1 are connected to stake pins for general use. TMROUT1 is connected to a stake pin. TMROUT0 is used for baud rate generation.

4.2.3 BUS STRUCTURE

The internal bus structure of the iSBC 186/51S board is shown in Figure 4-3. The primary internal bus of the board is the AD bus, a multiplexed address data bus which ties the 82586 Microprocessor and 80130A processor together.

The addresses put on the AD bus are latched by ALE (Address Latch Enable) at address latches U48, U45 and U61. The output of those latches is an address bus, designated the A BUS. The A BUS is connected directly to the 28-pin Local Memory Site located at U32/U49, U33/U50 and U34/U51. The A BUS is also connected to a Bus Latching Transceiver (BLT) at U60. The BLT connects the A BUS to the AB BUS, the dual-port RAM address bus and to the ADDR BUS, the MULTIBUS address bus.

During ALE times the AD BUS is an address bus. At times other than ALE the AD BUS is a data bus. The AD BUS, as a data bus, is connected through another BLT, located at U63, to the dual port memory array as the DB BUS. Through the same BLT the AD BUS is also connected to the MULTIBUS data bus, the DAT BUS.

The AD BUS is also buffered by two 8304 Octal bus Transceivers, at U43 and U44 to create a local data bus designated the D BUS. The D BUS is connected to the iSBX interface connectors, the flag byte logic, the Ethernet Mode address PROM, the 8274 Multi-Protocol Serial Controller and the 8283 Octal Latch.

Finally the AD BUS is connected directly to the 28-pin Local Memory Site.

4.2.4 I/O SELECT LOGIC

The I/O select logic is made up of a 16L8 PAL (Programmable Array Logic) device located at U41 and a 74LS138 3-to-8 Line Decoder/Multiplexer U27. The PCS1 (Peripheral Chip Select 1) line from the 80186 Microprocessor is used to identify an on-board I/O cycle.

The PAL device generates up to four iSBX chip selects, which can be either 8 or 16-bit standard addresses. The PAL also creates the chip selects for the 80130A I/O Section, the 8274 Multi-Protocol Controller and the Ethernet Station Address PROM. The PAL uses address bits 0, 4, 5 and 6 as well as BHE/ from the 80186

Microprocessor via the address latches to generate the chip selects.

An enable signal (CX) from the PAL is sent to the 74S138 device for all I/O addresses between 00C0(H) and 00CF(H). The 74S138 decodes those addresses to generate eight additional chip selects for the remaining I/O functions or the board.

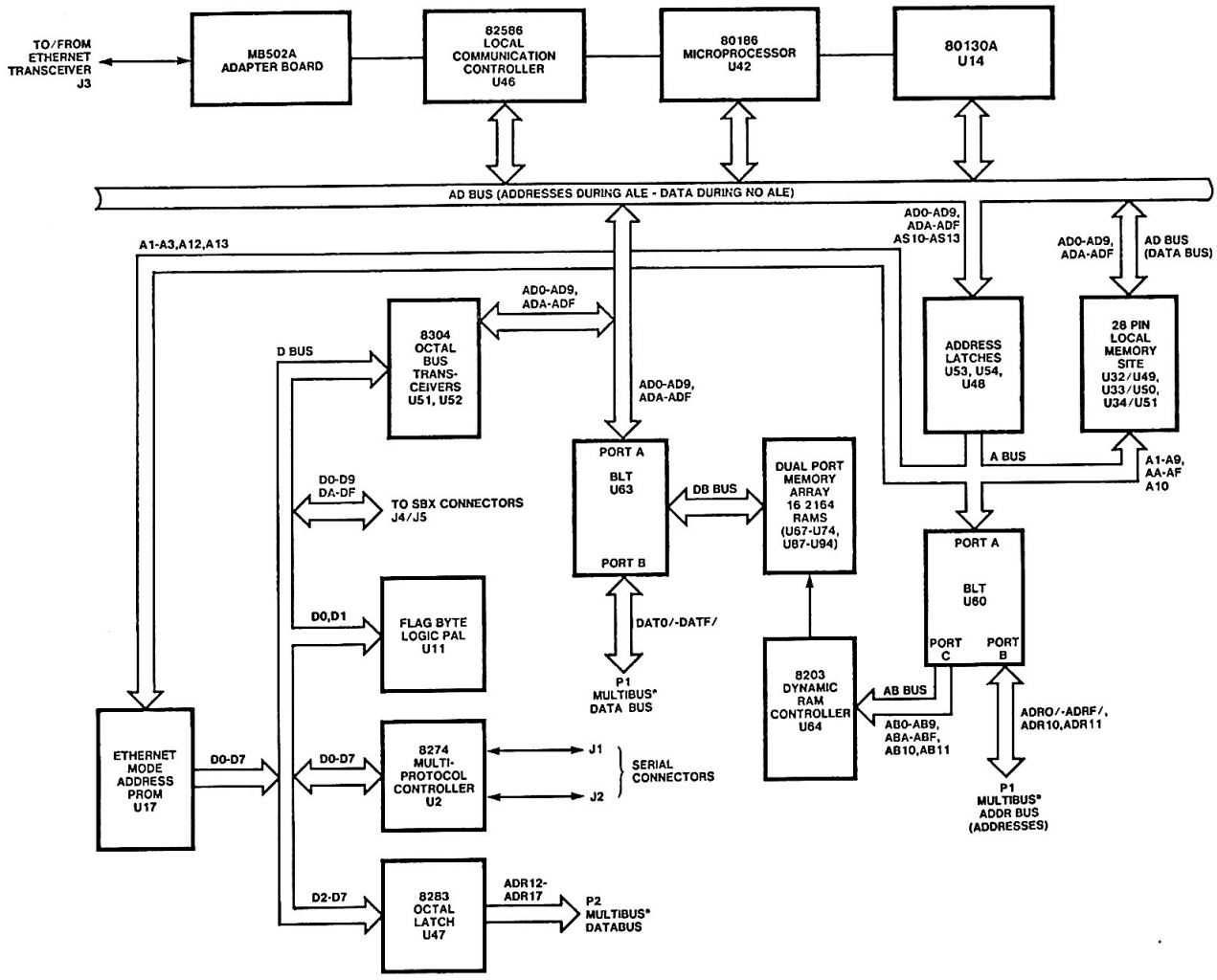


Figure 4-3. iSBC® 186/51S Board Internal Bus Structure

4.2.5 ETHERNET INTERFACE

The Ethernet interface is made up of an 82586 Local Communications Controller (LCC) and a MB502A Adapter Board, schematic Figure 5-3 in Section 5.

The MB502A Adapter Board ties the 82586 LCC to an external (to the iSBC 186/51S board) transceiver. The primary function of the MB502A is to provide the transmit clock (10MHz) to the LCC; to convert the received differential Manchester data from the external transceiver to single ended NRZ data for the LCC; to generate the carrier sense and collision detect signals for the LCC and to convert NRZ data from the LCC to Manchester differential data for transmittal to the external transceiver.

The carrier sense signal (XCD at P1-6) informs the LCC there is activity on the Ethernet cable. The collision detect signal (XCOL) informs the LCC that a collision is occurring on the Ethernet line. XCOL is passed through a delay/line to ensure that the collision detect input to the LCC remain active for at least two clock cycles.

The 82586 LCC is a highly integrated processor which assumes, for the Ethernet input, much of the load for the 80186 Microprocessor. It shares with the 80186 processor the AD BUS. The 80186, however, does determine priority between itself and the 82586 LCC. The 82586 requests access and the 80186 grants access. The 80186 can revoke the access at any time.

The 82586 LCC can access the local EPROM space and dual port memory. It cannot access the I/O interface.

4.2.6 MULTIBUS® INTERFACE

The iSBC 186/51S board can be operated as either a slave or a MULTIBUS master. When used as a master, an 8288 Bus Controller and an 8289 Bus Arbiter are used to control interface to the MULTIBUS. Common bus request, lock, parallel or serial priorities are all supported.

The board's 80186 processor AD BUS is interfaced to the MULTIBUS data bus through a bus latching transceiver (BLT) at U60. The fifteen lower address lines are also supplied to the MULTIBUS address bus through a second BLT at U63. The next three address lines ADRF/, ADR10/ and ADR11/ are also sent through the BLT, but in addition are buffered and applied to an address translation PROM located at U82. In a master mode operation, the buffered addresses are not used and the three address lines are only applied to the MULTIBUS interface. In slave mode operation, the address translation EPROM modifies the three address lines to determine if the MULTIBUS address is in the range of the dual port RAM mapping on the iSBC 186/51S board. If the address is in range, the MULTIBUS addresses are translated so they map into the appropriate dual port RAM addresses.

The upper six address lines (ADR12 through ADR17) can be driven by one of two sources, depending on whether the 16M Byte or 1M Byte space is to be used. A signal called window enable (WINDOW EN) determines which source will do the driving. WINDOW EN is the result of ORing the middle chip selects MCS0-MCS3 of the 80186 processor. Ordinarily these chip selects should be programmed in the 80186 to be each 64K Bytes in size and would start at local address 80000H. Thus for any access in the 80000(H) to 0BFFFF(H) range the window enable signal would be active. If the window enable signal is not active, the top four address lines (ADR14 through ADR17) are not driven and are held at logical "0". The other two address lines ADR12 and ADR13 are the latched address lines from the on-board AD BUS buffered by a 74LS240 buffer, located at U79.

When the window enable signal is active, six data bits (D2-D7) applied to 16M Byte Upper Address Latch U47 are transferred to the MULTIBUS as address bits ADR12 through ADR17. Thus, the iSBC 186/51S can access all MULTIBUS memory in the 16M Byte address space.

The bus clock (BCLK/) and constant clock (CCLK/) can be jumpered to the MULTIBUS interface. When so jumpered they are driven out-of-phase to reduce noise on the MULTIBUS lines.

4.2.7 SLAVE ADDRESSING

When the iSBC 186/51S board is used as a MULTIBUS slave, a decoding circuit decodes the MULTIBUS address for dual-port RAM access. The decoding circuit first determines if the MULTIBUS address is in the range of dual port mapping for the particular board being accessed. If the MULTIBUS address is within the mapping address range, the address is translated to the appropriate dual port RAM address. Two sets of jumpers on the Address Translation EPROM select the amount of dual port RAM and the top dual port RAM address visible to the MULTIBUS interface. The amount of dual port RAM visible to the MULTIBUS interface is always located in the upper addresses of the dual port RAM, as seen by the Processor. If one-half of the dual port RAM is visible to the MULTIBUS interface it is the upper half.

The slave addressing decode circuit is discussed in greater detail in paragraph 4.3.6.

4.2.8 iSBX™ INTERFACES

The iSBX bus is an extension of the local internal bus. This bus is interfaced to optional plug-in modules with a single iSBX connector. Two such connectors reside on the iSBC 186/51S board (J4 and J5). Connector J5 cannot be used with the MB502A board installed. All necessary power lines, data lines, and control lines are routed through the two iSBX connectors. All functions of the iSBX bus are supported by the iSBC 186/51S board except MULTIMODULE present (MPST/) and terminate DMA (TDMA). The TDMA signal from both iSBX MULTIMODULES are tied to stake pins and are available to users to support iSBX systems requiring these signals. The counter/timers are built into the 80186 and the 80130A devices. Two DMA channels are provided on the 80186.

The MWAIT/ functions for both normal and DMA operations are available.

The 80186 Processor on the iSBC 186/51S board treats the iSBX boards as another on-board I/O location. Pin assignments and signal descriptions for the iSBX bus connectors are given in Section 2. For additional iSBX MULTIMODULE information, refer to the Intel iSBX Bus Specification, Order No. 142686-002.

4.2.9 SERIAL CHANNELS

The iSBC 186/51S board uses an 8274 Multi-Protocol Controller, located at U2 to provide two channels of serial I/O. By the use of jumpers, Channel A, connector J1, can be setup to have an RS232C or RS422A/449 interface. In the RS232C configuration either a DTE (Data Terminal Equipment) or DCE (Data Communication Equipment) interface is possible. In the RS422A/449 configuration only DCE is available. Channel B is RS232C and DCE only.

In the RS422A/449 configuration (Channel A) the output drivers can be three-stated to allow multidrop networks.

Operation of the 8274 controller is described in detail in paragraph 4.3.10. Configuring of the serial channels is described in Section 2 of this manual.

4.2.10 LOCAL MEMORY

The iSBC 186/51S board provides a 28-pin local memory site consisting of six 28-pin JEDEC connectors. The six connectors are arranged in three pairs to allow an 8 or 16-bit bus. The site can be configured to accept a mix of user supplied ROM, PROM, RAM, and iRAM memory devices. Device capacities can be either 4, 8, 16 or 32K. Device types can be mixed between site connector pairs; device capacities and devices types must remain the same within a pair.

A stake pin matrix allows configuring the local memory for all specified memory devices. Stake pin configuration is described in Section 2 of this manual.

The local memory select logic determines the address range of the local memory and generates the control signals for the memory. Paragraph 4.3.9 discusses in detail the local memory and the local memory select logic.

4.2.11 DUAL PORT RAM

The dual port RAM consists of 16 2164 dynamic RAMs, an 8203 Dynamic RAM Controller and the dual port RAM control logic. The dual port memory size is 128K Bytes, expandable to 256K Bytes with an optional iSBC 304 Memory Expansion MULTIMODULE.

The dual port RAM exists at the bottom, lowest local address, of the 80186 processor. The local address range of the dual port RAM is 0000(H) through 1FFFF(H). With the iSBC 304 MULTIMODULE installed the local address range becomes 0000(H) through 3FFFF(H).

The 8203 Dynamic RAM Controller provides all control and timing signals required for operation of the memory array. Refresh requests on the 8203 controller can be jumpered to ground or to a pin on the MULTIBUS P2 connector (for testing purposes). In the "as shipped" configuration the refresh request pin is jumpered to ground causing refresh requests to be automatically generated by the 8203 controller.

The dual port control logic determines whether the 80186 processor, the 82586 LCC on the MULTIBUS Interface has access to the dual port RAM. Paragraph 4.3.8 describes in detail operation of the dual port control logic.

4.2.12 80130A INPUT/OUTPUT

The 80130A device on the board is used for its timers and as the master interrupt controller. The delay and baud timers of the 80130A are terminated at stake pins. The 80130A provides the interrupt vector for all interrupts except the 80186 interrupt (INT2) and the 8274 interrupt (8274 INT). These two interrupts are treated as local interrupts with the 80186 processor or the 8274 controller providing the vector.

The 80130A is internally divided into a control unit (CU) and an operating system unit (OSU). The OSU contains facilities for OSP Kernel support including the system timers for scheduling and timing waits and the interrupt controller for interrupt management support.

The Programmable Interrupt Controller (PIC) is an integral unit of the 80130A. Its eight input pins handle eight vectored priority interrupts. One of these interrupt pins, IR2, is used for the SYSTICK time function in timing waits. During the 80130A initialization and configuration sequence, each 80130A interrupt pin is individually programmed as either level or edge sensitive.

In addition to standard PIC functions, the 80130A PIC unit has an LIR/ output signal, which when low indicates an interrupt acknowledge cycle.

For detailed information on the 80130A device, see the iAPX 86/30 (80130A) Operating System Processor Data Sheet, Order Number 210216.

4.2.13 DEDICATED PARALLEL I/O

The dedicated parallel I/O block on the iSBC 186/51S board consists of a 74LS279 Programmable Latch and a 74LS244 Line Driver.

The 74LS279 latch is used to create eight parallel output bits which are dedicated for on-board functions. Table 4-1 shows the data written and the functions enabled by the 74LS259 latch.

Four parallel inputs, which can be read by the 80186 processor are available. These four inputs are all tied to +5 volts, but can be jumpered to ground, thus permitting them to define a preset system configuration. For example, if two sets of software existed on the board, an installed jumper could be used to inform the 80186 which software set to run.

The four input lines are also jumperable to the outputs of 74LS279 latch at U7. The latch outputs can indicate if a timeout has occurred (stake pin E127) and if so, whether the board timed out waiting for the MULTIBUS (stake pin E121) or if the board timed out on the MULTIBUS. A third latch output can indicate that a software reset has occurred (stake pin E125). A separate jumper input (stake pin E132) indicates that the iSBC 304 Memory Expansion MULTIMODULE is installed. To read these inputs the 80186 processor does a byte I/O read of the 74LS244 at U35.

4.2.14 FLAG BYTE SIGNALLING

The iSBC 186/51S board uses a method called flag byte for interrupt signaling between the on-board 80186 processor and a MULTIBUS processor. Flag byte is I/O mapped from both the on-board processors and the MULTIBUS. Data written to the

address selected determines what action is taken. The MULTIBUS I/O address selected is determined by the installation of three jumpers. The addresses which are selectable for either 8-bit or 16-bit data transfers are shown in Table 4-2.

Table 4-2 shows the flag byte signaling codes and the actions they cause to be generated. The codes can be written by the 80186 (data bits D0, D1 and D2) or the MULTIBUS interface (data bits DAT0, DAT1 and DAT2).

Table 4-1. Parallel Output Programming, 74LS259 Latch, U26

Data Written	Function Performed
00(H)*	LOOPBACK ESI/ (active low) – Enable loopback Ethernet Channel at MB502A Adaptor Board.
01(H)*	Not Used.
02(H)*	NMI EN (inactive low) – Disable Non-Maskable Interrupts.
03(H)*	OVERRIDE (active high) – Disable MULTIBUS Locked override.
04(H)*	NVEN (inactive low) – Disable Non-Volatile RAMs.
05(H)*	MB INT (inactive low) – Turn off MULTIBUS Interrupt.
06(H)*	U26-11 (inactive low) – Turn off diagnostic LED, DS3.
07(H)*	U26-12 (inactive low) – Turn off diagnostic LED, DS2.
08(H)	LOOPBACK ESI/ (inactive high) – Disable loopback Ethernet Channel at MB502A Adaptor Board.
09(H)	Not Used.
OA(H)	NMI EN (active high) – Enable Non-Maskable Interrupts.
OB(H)	OVERRIDE (inactive low) – Enable MULTIBUS locked override.
OC(H)	NVEN (active high) – Enable Non-Volatile RAMs.
OD(H)	MB INT (active high) – Turn on MULTIBUS Interrupt.
OE(H)	U26-11 (active high) – Turn on diagnostic LED, DS3.
OF(H)	U26-12 (active high) – Turn on diagnostic LED, DS2.

* Default condition on reset.

Table 4-2. Flag Byte Selectable MULTIBUS® Addresses

8-Bit Data Transfer Addresses (Hex)	E209-E205	E213-E209	E210-E206	E211-E207	E212-E208
A4	X	-	X	X	X
A5	X	-	X	X	-
A6	X	-	X	-	X
A7	X	-	X	-	-
A4	X	-	-	X	X
A5	X	-	-	X	-
A6	X	-	-	-	X
A7	X	-	-	-	-
16-Bit Data Transfer Addresses (Hex)	**E209-E205**	**E213-E209**	**E210-E206**	**E211-E207**	**E212-E208**
08A4	-	X	X	X	X
08A5	-	X	X	X	-
08A6	-	X	X	-	X
08A7	-	X	X	-	-
09A4	-	X	-	X	X
09A5	-	X	-	X	-
09A6	-	X	-	-	X
09A7	-	X	-	-	-

X = Jumper Installed
- = Jumper Not Installed

Table 4-3. Flag Byte Signaling Codes

80186 Codes			MULTIBUS Codes			Action
D2	D1	D0	DAT2	DAT1	DAT0	
1	0	0	-	-	-	Clear interrupt to iSBC 186/51S
-	-	-	1	0	0	Clear interrupt to MULTIBUS
0	1	0	-	-	-	Set interrupt to MULTIBUS
-	-	-	0	1	0	Set interrupt to iSBC 186/51S
0	0	1	-	-	-	Clear Interrupt to MULTIBUS
-	-	-	0	0	1	Reset iSBC 186/51S

NOTE: All other codes are illegal. Reading port from either side will yield indeterminate data.

4.3 Circuit Descriptions

The circuit descriptions in the following paragraphs provide more detailed information on the internal operation of the iSBC 186/51S board. The schematic diagram for the iSBC 186/51S is provided as Figure 5-3.

Both active high and active low signals are used. A signal mnemonic that ends with a slash (e.g. DAT7/) denotes a signal active in the low state (less than 0.4 volts). Conversely, a signal mnemonic without a slash (e.g. ALE) denotes a signal active in the high state (greater than 2.0 volts).

4.3.1 POWER-UP INITIALIZATION

When INIT/ is applied to the iSBC 186/51S Board RESET/ (sheet 2 of Figure 5-3), is driven active low. RESET/ active resets the 80186 microprocessor (U42) and causes it to generate RST OUT high. RST OUT resets the 82586 LCC at U46. RESET/ after buffering and inversion becomes RESET.

RESET active resets any iSBX modules connected to the iSBC 186/51S through connectors J4 and J5.

RESET/ initializes the 8289 Bus Arbiter at U58. After initialization the arbiter does not have the use of the system bus. RESET/ resets the 8274 Multi-Protocol Serial Controller at U2 forcing it to an idle state. The controller will remain idle until the control registers are loaded. RESET/ also resets the program latch at U26 which provides on-board status inputs to the 80186 processor. RESET/ clears the latch so all outputs go to the zero state.

The initialization just described can be performed at any time by activating the AUX RESET/ signal via MULTIBUS auxiliary connector P2, pin 38.

4.3.2 80186 MICROPROCESSOR CIRCUITS

The 80186 Microprocessor is internally divided into two processors, the Bus Interface Unit (BIU) and an Execution Unit (EU). The BIU is used to constantly

monitor EU and an internal queue for memory or I/O operations. Each time the BIU accesses the iSBC 186/51S board's internal bus, the 80186 must execute at least four major cycles, called T-States. The timing required for each T-State is discussed in the following paragraphs.

The first T-State, T1 indicates the type of access and the location of the transfer source or destination. The 80186 activates its status lines S0/, S1/, and S2/, indicating the type of operation to be performed for the up-coming cycle. The operations defined by the status bits are as shown below:

S2/	S1/	S0/	Cycle
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1	0	0	Code Access
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive

0 = Low State, 1 = High State

When the status bits are asserted the 8288 Bus Controller located at U25 will activate its Address Latch Enable (ALE) line. While ALE is active the address for the bus cycle is placed on the AD BUS by the 80186 (Figure 4-3). Before the end of T1, ALE goes inactive and the address is latched.

ALE through the PROM Control PAL at U38 (Table 4-19) generates T22 and T22/. T22 is low when ALE is active. T22/ is high when ALE is low. T22 disables commands from the 8288 controller at U25 until the rising edge of T2. The 8288 controller at U81 will be held disabled during an on-board operation by ON BD ADDR/ active and AEN/, from the 8289 Bus Arbiter, inactive.

During the T2 State the address presented during T1 is removed from the AD BUS. Any one of four bus cycles can be performed during T2, following removal of the address; read cycle, write cycle, interrupt acknowledge cycle and halt or passive cycles.

If a read cycle is being performed either MEMRD/ (MRDC/) or IORD/ (IORC/) becomes active from one of the bus controllers. The 80186 removes its address from the AD BUS and sets the lines to the receive mode. The chip enable terms are activated by the PAL devices if the address is a valid on-board location. The 8288 Controller (U25) by generating ONBD DT/Rlow, and DEN high enable determines data flow through the 8304 Data Transceivers and the data BLT (63).

During a write cycle the 80186 drives the data lines. After the address is removed, the data is put on the AD BUS. The 8288 command AMWC/ (MEM WT/) or AIOWC/ (IOWT/) and the chip enable terms become active as during a read cycle. The 8288 Controller activates the DEN signal for the transfer.

The interrupt acknowledge cycles for the 80186 are described in paragraphs 4.4.2 and 4.4.3.

If a HALT or PASSIVE state is indicated on the status lines, no commands will be issued. Chip enable terms will still be generated and data integrity will be maintained.

During the T3 state, the data transfer is complete if the access time of the peripheral has been met.

During the T4 state, all command lines are placed in their inactive states. All control and direction lines also become inactive, until the status lines are asserted.

An 80186 hold is initiated when another processor, the 82586 LCC, is requesting the local bus. The HOLD input to the 80186 is asserted high. The 80186 issues a HLDA (Hold Acknowledge) to the 82586 LCC. Simultaneous with the issuance of HLDA the 80186 will float the local bus and control lines. After HOLD is detected as being low, the 80186 will lower HLDA. When the 80186 needs to run another bus cycle, it will again drive the local bus and control lines.

The internal ready capability of the 80186 processor is unused in the iSBC 186/51S application. The 80186 ready is generated by Ready Logic PAL U40. PAL programming is shown in Table 4-4.

Table 4-4. Ready Logic PAL U40 Programming

1. IM BUS AEN (L) = BUS MASTER ADEN (L) + WINDOW EN (H)

2. WINDOW AEN (L) = BUS MASTER ADEN (L) + WINDOW EN (L)

NOTE
BORT is PAL output U40-15

3. BORT (H) = (BUS MASTER ADEN (H) · XACK (L))
+ TIMEOUT (L)
+ (PCS1 (L) · WAIT (L))

NOTE
BORT 2 is PAL output U40-15 and PAL input U40-19. WAIT is PAL input U40-5.

4. READY (H) = BORT 2 (H)
+ (ON BD CMD (L) · CAS (L))
+ (ON BD CMD (L) · DPXACK (L))
+ (ON BD DPREQ (H) · ON BD ADDR (L) · WAIT (L) · PROM RDY (H) · PWT (H))

READY will be generated active for the following conditions:

- As a bus master ready when BUS MASTER ADEN is active, ALE from Bus Controller U81 is inactive, AEN from Bus Arbiter U58 is active, and XACK/ from the MULTIBUS is active.

- When accessing on-board I/O, PCS1 from the 80186 processor is active high and WAIT is inactive, WAIT is the result of ANDing MWAIT1/ high, MWAIT2/ high and Interrupt Wait, PAL output U30-14, high.

- READY will be generated active if stake pins E34 and E35 are tied together and a timeout occurs, TIMEOUT/ low.

- When accessing dual port RAM using ONBDCMD/, generated by PAL U56 indicating that the on-board processor has the dual port. CAS/ (Column Address Strobe) and DPXACK/ from the 8203 Controller in the dual port overlap. CAS/ becomes active before dual port RAM data is valid. By the time the 80186 processor or the 82586 LCC can respond to CAS/ the data is valid.

- READY/ active will be generated for local memory accesses by ONBDDPREQ/ inactive, ONBDADDR/ active, WAIT inactive (the result of ANDing MWAIT/ high, MWAIT2/ high and Interrupt Wait, PAL output U31-14 high) and PROM RDY high.

Ready Logic PAL U40 also generates two other signals IM BUS AEN/ and WINDOW AEN/. These two signals can not be active at the same time, since IM BUS AEN requires that WINDOW EN, the result of ORing the MSC0 through MSC3 outputs of the 80186 processor, be active high and WINDOW AEN/ requires that WINDOW EN be inactive low.

IM BUS AEN/ active and WINDOW AEN/ allow the iSBC 186/51S board to view the MULTIBUS interface as either a 256K Byte or 16M Byte address space. When IM BUS AEN/ is active and WINDOW AEN/ is inactive the MULTIBUS interface is viewed as a 1M Byte address space, the 8283 16M Byte Upper Address Latch (sheet 10 of Figure 5-3) is disabled and its address lines placed in a high impedance state. If IM BUS AEN/ is inactive and WINDOW AEN/ is active, the 8283 is enabled and its outputs select a 256K Byte address space in the 16M Byte MULTIBUS address range.

For detailed information on the 80186 Microprocessor see the iAPX 186 High Integration 16-Bit Microprocessor Data Sheet, Order Number 210451.

4.3.3 I/O SELECT LOGIC

The I/O select logic consists of a 16L8 PAL device at U41 and a 74S138 3-to-8 line decoder at U27. PCS1/ from the 80186 microprocessor identifies an on-board I/O cycle. The PAL device creates four iSBX chip selects (SBX1 CS0/, SBX1 CS1/,

SBX2 CS0/ and SBX2 CS1/. The iSBX chip selects can be either 8 or 16-bit standard addresses as determined by a jumper installed between E192 and E200 or between E200 and E204. If E192-E200 is not installed, the iSBX1 chip selects are 8-bit standard addresses. If E192-E200 is installed, the iSBX1 chip selects are 16-bit standard addresses. If E200-E204 is not installed, the iSBX2 chip selects are 8-bit standard addresses. If E200-E204 is installed, the iSBX2 chip selects are 16-bit standard addresses.

The PAL device creates the iSBX chip selects from address bits A0, A3, A4, A5, A6, BHE/ (Byte High Enable), and PCS1. The PAL also creates the chip selects for the 80130A I/O section (80130A I/O CS/), the 8274 Multi-Protocol Serial Controller and the station address PROM (NODE ADDR SEL/) located at U17.

The PAL device also generates an enable signal to the 74S138 decoder for I/O addresses C8(H), CB(H), CC(H), CE(H), D0(H), D2(H), D4(H), and D6(H). The decoder using address bits A1, A2 and A3 decodes eight more chip selects for the remaining I/O functions on the board. The chip selects generated by the decoder and their function are shown below:

Chip Selects	Function
EDGE RESET CS/	Resets the 74S279 at U7 in the dedicated parallel I/O circuits, reference paragraph 4.3.11.
CONFIG CS/	Enables the 74LS244 configuration buffer/driver at U35. The buffer supplies user defined board configuration data to the 80186 processor.
LATCH CS/	Enables the 74LS259 programmable latch at U26. The latch is used to create eight dedicated output latches. The data on the data bus gets strobed into the latch with the trailing edge of LATCH CS/.
82D2E CA/	This signal, after inversion, is the channel attention input to the 82586 LCC, located at U46.
MDACK2/	This signal is generated to the iSBX MULTIMODULE board at connector J4 and acknowledges the requested DMA cycle has been granted.

Chip Selects	Function
MDACK1/	This signal is generated to the iSBX MULTIMODULE board at connector J5 and acknowledges the requested DMA cycle has been granted.
WINDOW LATCH CS	Strobes the processor address bits A2 through A7 into the 8283 Window Latch at U47. The window latch permits any one megabyte of the 16 megabyte MULTIBUS address to be addressed by the iSBC 186/51S.

Programming for the chip select decoder PAL at U41 is shown in Table 4-5.

Table 4-5. Chip Select Decoder PAL U41 Programming

1. SBX1 CS0 (L) = PCS1 (L) · A6(L) · A5(L) · A4(L) · A0(L)

NOTE

SBX1 SEL is PAL input U41-7 (E200-E192 installed).

2. SBX1 CS1 (L) = (PCS1(L) · A6(L) · A5(L) · A4(L) · A0(L)
· BHE(L) · SBX1 SEL(L))
+ (PCS1(L) · A6(L) · A5(L) · A4(L)
· A0(H) · SBX1 SEL(L) · BHE(L))
+ (PCS1(L) · A6(L) · A5(L) · A4(H)
· A0(L) · SBX1 SEL(H))

3. SBX2 CS0 (L) = PCS1(L) · A6(L) · A5(H) · A4(L) · A0(L)

NOTE

SBX2 SEL is PAL input U41-8 (E200-E192 installed).

Table 4-5. Chip Select Decoder PAL U41 Programming (Cont'd.)

4. SBX2 CS1(L) = (PCS1(L) · A6(L) · A5(H) · A4(L) ·
A0(L) · BHE(L) · SBX2 SEL(L))
+ (PCS1(L) · A6(L) · A5(H) · A4(L)
· A0(H) · SBX2 SEL(L) · BHE(L))
+ (PCS1(L) · A6(L) · A5(H) · A4(H)
A0(L) · SBX2 SEL(H))

5. 80130A I/OSEL (L) = PCS1(L) · A6(H) · A5(H) · A4(L) · BHE(H) · A0(L))

NOTE
8274CS is the U41-17 output of PAL U41.

6. 8274CS (L) = PCS1(L) · A6(H) · A5(L) · A4(H) · A3(H)

NOTE
CX is the U41-18 output of PAL U41.

7. CX (L) = (PSC1(L) · A6(H) · A5(L) · A4(L) · A3(H))
+ (PSC1(L) · A6(H) · A5(L) · A4(H) · A3(L))

8. NODE ADDR SEL (L) = PCS1(L) · A6(H) · A5(H)
· A4(H) · IORD(L)

4.3.4 ETHERNET INTERFACE CIRCUITS

The Ethernet interface consists of an MB502A Adaptor Board and a 82586 Local Communications Controller. The interface is shown on sheet 2 of schematic 146643.

The MB502A Adaptor Board is tied to the iSBC 186/51S board through the IC socket located at U31 on the iSBC 186/51S Board. The MB502A performs five basic functions:

- It generates the transmit clock (TXC/) to the 82586 Controller.

- It generates the carrier sense and collision detect signals for the 82586 from receive pair and collision pair signals generated by the external transceiver.

- It converts the received differential Manchester data from the external transceiver to single-ended NRZ data.

- It provides the received data clock.

- It converts the single-ended transmitted NRZ data from the 8258 Controller to Manchester differential data for transmittal to the external transceiver.

The primary element of the MB502A Adaptor Board is a Fujitsu, MB502A Ethernet Encoder/Decoder integrated circuit. An internal oscillator in the IC generates a 100 Mhz output. That output processed by an external 100 MHz crystal and tank circu is returned to the IC. The IC divides the returned oscillator output by 10 to provide a 10 MHz clock TCKN (TXC) to the 82586 LCC. This same 10 MHz clock is also used as the MULTIBUS bus clock (B CLK), constant clock (CCLK) and Multimodule clock (MCLK).

The collision input signal is a 10 MHz $\pm$ 15% square wave generated by the externa transceiver, whenever two data frames are superimposed in the coaxial cable. When a valid collision-presence signal is present (COLLISION $\pm$, pins U31-11/P1-11 and U31-12/P1-12) the MB502A generates XCD/ (Carrier Sense) active to the 82586 LCC indicating activity in the coax cable.

When XCD/ is active the 82586 Controller defers to the passing data packet by delaying any pending transmission of its own. After XCD/ becomes inactive the 82586 continues to defer for 96 TXC/ units. At the end of this time if a packet is ready for transmission the 82586 initiates a transmission independent of the Carrier Sense Signal.

When a collision is detected during a packet transmission, the transmission is continued with at least 32 bits, but no more than 48 additional bits. This jam ensures detection of the collision by all stations on the Ethernet. The contents of the jam are all "1s".

The 82586 LCC retransmits after the collision, without notifying the user. If another collision occurs it retransmits again and repeats the transmissions a maximum of 15 times. If collisions are still occurring, the retransmission stops and the user notified.

The 82586 LCC upon command (CA, Channel Attention) reception from the 80186 CPU moves data from memory, gains access to the serial link (through the MB502A and Ethernet Transceiver), formats the data into packets and targets the packets to their destination.

The receive process after being commanded by the 80186 proceeds without further Intervention of the 80186 processor. During the receive process, data pockets are detected, addresses checked and data moved to memory. Both commands and buffers used by the 82586 are memory resident.

The 82586 is reset when RST goes high. Receipt of RST will immediately stop any 82586 activity. Resetting of the 82586 will be done within 10 system clock cycles from RST high. When RST goes low the 82586 LCC waits for the first channel attention command (82586 CA/) before starting its initialization sequence.

The first 82586 CA/ after RST begins the initialization sequence beginning at location 0FFFFF6(H). All following 82586 CA/ signals cause the 82586 to begin execution of new command sequences.

The shared data bus of the 82586 LCC and the 80186 processor is sixteen bits wide. The board's on-board memory could be accessed simultaneously by the 82586 and the 80186. Bus contention is prevented by two signals HOLD generated by the 82586 and HLDA (Hold Acknowledge) generated by the 80186.

When the 82586 requires the local bus it generates HOLD active high to the 80186. At the end of its current bus cycle the 80186 gives up the bus to the 82586 and

generates HLDA high to the 82586. The 80186 can withdraw its grant of the bus by dropping HLDA low. If HLDA is dropped low the 82586 will drop HOLD low within three bus cycles.

The status outputs, S0/ and S1/, of the 82586 define the type memory transfer during a memory cycle. Because the 82586 does not have I/O access capability only two status bits are needed. The encoding of the status signals are shown below:

S1/	S0/	Cycle
0	0	Not Used
0	1	Read Memory
1	0	Write Memory
1	1	Passive

The status outputs are enabled from the middle of T4 to the end of T2. They are returned to the passive state during T3, or during a TW state when ARDY is high.

S0/ and S1/ are applied to an 8288 Bus Controller located at U25. The Bus Controller uses these signals to generate all memory timing and control signals. Any change of the status signals from the passive state signals the Bus Controller to begin the next T1 to T4 bus cycle.

The BHE/ (Byte High Enable) output of the 82586 is tied to the same output of the 80186 and becomes S7/BHE. This signal enables data onto the most significant half of the data bus at several locations on the iSBC 186/51S board.

Timing parameters for the 82586 LCC device can be found in the 82586 Reference Manual, Order Number 210891.

4.3.5 STATION ADDRESS PROM

The Ethernet station address is stored in a 74S288 256-bit PROM located at U17 on the iSBC 186/51S board. This address is read by the on-board processor and passed

to the 82586 LCC during the initialization sequence as described in Chapter 3. Each board is read by the on-board processor and passed to the 82586 LCC during the initialization sequence as described in Chapter 3. Each board has a unique address stored in the station address PROM.

The 74S288 PROM is a 32-byte (8 bits each) device. Only eight bytes are allowed to be read. The upper address lines ADE and ADD are tied to status LED's DS2 (ADE) and DS3 (ADD). When both LEDs are off, the Ethernet address can be read from the PROM.

The first six bytes (octets) are the unique 48-bit Ethernet station address. The station's physical address is distinct from the physical address of any other station on any Ethernet. The seventh and eighth bytes from the PROM are both zero.

The first bit of a data link address distinguishes physical from multicast addresses; 0 equals a physical address; 1 equals a multicast address. In either case, the remainder of the first octet and all subsequent octets form a 47-bit pattern.

As read from the 74S288 PROM the Ethernet address format is as follows:

Byte	Hex Value	Octet/Byte
F0	00	1
F2	AA	2
F4	00	3
F6	00 (UU)	4
F8	01 (UU)	5
FA	FF (UU)	6
FC	00	7
FE	00	8

NOTE

The address shown above is a unique Ethernet address. The bytes designated (UU) are variable depending on the iSBC 186/51S board and address PROM being considered.

The unique address being considered corresponds to the following sequence of bits on the Ethernet:

(0)	(0)	(A)	(A)	(0)	(0)
0000	0000	0101	0101	0000	0000
(0)	(0)	(1)	(0)	(F)	(F)
0000	0000	1000	0000	1111	1111

where the bits are transmitted from left to right.

Because the station address PROM is an 8-bit device on a 16-bit bus, the data appears on even addresses in the station address PROM address range. Only byte I/O reads are performed on the PROM at Ethernet station addresses 00F0-00FE.

The PROM is selected by MODE ADDR SEL/going low. This signal is generated by chip select PAL U41 in the I/0 select logic, see paragraph 4.3.3 and Table 4-5 for circuit operation.

The Ethernet processor addresses are controlled by the Ethernet Address Administrator as described in paragraph 2-11 of this manual. While the Ethernet station address in the 74S288 PROM can not be changed, the user can obtain, via the Ethernet Address Administrator, his own address and store it in the local memory, the 28-pin JEDEC site of the iSBC 186/51S board. This address can be read by the on-board processor and passed to the 82586 LCC during initialization.

4.3.6 MULTIBUS® INTERFACE CIRCUITS

The iSBC 186/51S board can be either a MULTIBUS master or a MULTIBUS slave. As a master an 8288 Bus Controller and 8289 Bus Arbiter interface to the MULTIBUS. Address and data are transferred to the MULTIBUS interface through two bus latching transceivers (BLTs). The BLTs used on the board are identical and are both enabled by a BLT Control PAL located at U62.

BLT Control PAL U62 generates three output signals: ADDREN/ (Address Enable), DPDEN/ (Dual Port Data Enable) and DBDCMD (Delayed Board Command).

ADDREN/ is applied to the data enable (DEN) pin of address BLT U60. When ADDREN/ is active low the drivers, in the BLT, for the selected data channel are enabled.

DPDEN/ is applied to the data enable (DEN) pin of data BLT U63. When DPDEN/ is active low the drivers, in the BLT, for the selected data channel are enabled.

DBDCMD/ is used to enable (DBDCMD low) or disable (DBDCMO high) a set of buffer inverters. These drivers are used to enable the drivers in the 8203 RAM Controller. Using the delayed board command (DBDCMD/) prevents the drivers disabling, in the 8203, at the same time as the address inputs to the 8203 change. If the changing occurs at the same time ringing may occur.

Programming for BLT Control PAL U62 is shown in Table 4-6.

The BLT is a 68-pin device capable of channeling 16 bits of data over three data ports while checking and generating parity (one parity bit per 8-bit byte). The BLT can also be strapped for non-parity operation passing 18 bits per port.

Table 4-6. BLT Control PROM U62 Programming

```
DBDCMD(L) = ONBDCMD(L)

ADDREN(L) = SLAVEMODE(H) + (BUSEN(L) - ALE(L))
            +DPACC (L) . ALE(L))

DATEN(L)  = DPWR(L)
            +(BUSDEN(H) + IORC(H) . MRDC(H)
            +(BUSDEN(H) . XACK(L))
            +(COMMAND(H) . DCAS(L)
            +(SLAVEMODE(H) . DCAS(L) . MRDC(L))
            +(SLAVEMODE(H) . DPXACK(L) . MRDC(L))
```

The BLT located at U60 channels address bits between the address latches at U45, U48 and U61, the local memory site at U32-U34/U49-U51, the dual port RAM array and the MULTIBUS interface. BLT U60 is configured, in this application for parity off, non-swap transfers. The channeling of addresses through the BLT is determined by the states of the SLAVE MODE/ signal and the BUS MASTER ADEN output of the 8288 Bus Controller located at U81. Table 4-7 shows the BLT transfer paths available in this application.

From Table 4-7 it should be noted that with SLAVE MODE/ active low and BUS MASTER ADEN low address bits are transferred between the MULTIBUS interface and the dual port RAM. When BUS MASTER ADEN is high address bits are transferred between the MULTIBUS interface and the various functions of the board.

When SLAVE MODE/ is high and BUS MASTER ADEN is low address bits are transferred between the 80186 processor and the dual port RAM. When BUS MASTER ADEN is high the address bits are transferred between the 80186 and the MULTIBUS.

The data BLT located at U63 channels data bits between the 80186 microprocessor, the dual port RAM memory and the MULTIBUS interface. Channeling of data through the BLT is determined by the states of SLAVE MODE (SEL A/$\overline{B}$ on U63), BUS MASTER ADEN (DESTC on U63) and MULTIBUS DT/$\overline{R}$ (DT/$\overline{R}$ on U63). SLAVE MODE/ is generated in the dual-port arbitration logic. BUS MASTER ADEN is generated by the 8288 Bus Controller and the 8289 Bus Arbiter and MULTIBUS DT/$\overline{R}$ is generated by the dual port arbitration logic. Table 4-8 is a truth table for BLT U63 and shows the possible data transfer paths through the BLT.

The Bus Low Disable pin (BLD/) and Bus High Disable pins are used in this application. The BLD/ input when low disables the lower order data byte (bits DAT0 through DAT7) of either Port B or Port C, depending on the BLT configuration. The BHD/ input when low disables the higher order data byte (bits DAT8 through DATF) of either Port B or Port C, again depending on the BLT configuration. These two inputs cannot be active at the same time. The conditions required for an active BLD and BHD are as shown.

BLD/ Active	BHD/ Active
Local DPRD/ High and ABO High	BHEN/ High and ABO Low

When the board is being operated as a master, the 8288 Bus Controller (located at U81) and the 8289 Bus Arbiter are used to interface to the MULTIBUS. When the AEN/ output (pin U58-13) of the 8289 arbiter goes low and T22 goes low the 8288 controller has the system bus, providing ONBDADDR/ is inactive. The 8288 device will generate the memory read, memory write, I/O read and I/O write commands in accordance with the states of the status inputs S0/, S1/ and S2/. Table 4-9 shows the signal generation.

Table 4-7. Address BLT U60 Truth Table

SLAVE MODE/ (SEL A/B)	BUS MASTER ADEN (DESTC/)	+5V DT/R	PORTS		
			A (Address Latch)	B (MULTIBUS)	C (Dual Port RAM)
L	L	H	X	Input	Output
L	H	H	Output	Input	X
H	L	H	Input	X	Output
H	H	H	Input	Output	X

Table 4-8. Data BLT U63 Truth Table

SLAVE MODE/ (SEL A/$\overline{B}$	BUS MASTER ADEN (DESTC)	MULTIBUS (DT/$\overline{R}$	PORTS		
			A 80186	B (MULTIBUS)	C Dual Port RAM
L	L	L	X	Output	Input
L	L	H	X	Input	Output
L	H	L	Input	Output	X
L	H	H	Output	Input	X
H	L	L	Output	X	Input
H	L	H	Input	X	Output
H	H	L	Output	Input	X
H	H	H	Input	Output	X

Table 4-9. Bus Controller U81 Status Word

S2/	S1/	S0/	Processor State	Command Generated
L	L	L	Interrupt Acknowledge	Not Used
L	L	H	Read I/O Port	IORC/ MULTIBUS
L	H	L	Write I/O Port	IOWC/ MULTIBUS
L	H	H	Halt	No Command Generated
H	L	L	Code Access	MRDC/ MULTIBUS
H	L	H	Read Memory	MRDC/ MULTIBUS
H	H	L	Write Memory	MWTC/ MULTIBUS
H	H	H	Passive	No Command Generated

The 8289 Bus Arbiter can be configured by a user in several different modes by using the arbiter's associated jumpers. As delivered by the factory the jumpers are installed as shown on sheet 4 of schematic 146976, and summarized below:

E168 to E174 (BPRO/)
E175 to E183 (CBRQ/)
E130 to E131 (LOCK/)

In this configuration with ANYRQST (U58-14) held high, if CBRQ/ (Common Bus Request) is activated, the bus is surrendered at the end of the cycle being run. When the bus is surrendered, BREQ/ (Bus Request) is driven low. BUSY/ (U58-11) can be either an input or an output. When the arbiter has given the bus to the U81 controller, BUSY/ is made low pulling the MULTIBUS BUSY line low keeping all other arbiters on the bus off. When the U58 arbiter is done with the bus it makes BUSY/ high allowing another arbiter to acquire the multimaster bus.

When the MULTIBUS interface makes BPRN/ (Bus Priority In) active it instructs the arbiter that it may acquire the system bus on the falling edge of BCLK. BPRN/ indicates to the arbiter that it is the highest priority requesting arbiter on the bus. BPRN/ inactive instructs the arbiter that it has lost priority to a higher priority arbiter.

BREQ/ (Bus Request) is generated in response to status bits S0/, S1/ and S2/ as shown:

S0/	S1/	S2/	Response
L	L	H	BREQ/ (For Read I/O Port)
L	H	L	BREQ/ (For Write I/O Port)
H	L	H	BREQ/ (For Memory Read)
H	H	L	BREQ/ (For Memory Write)

If the jumper between E175 and E183 is removed and E183 is connected to E169 (ground) the 8289 arbiter is forced to surrender the multi-master system bus after each transfer cycle. When the surrender occurs, BREQ/ is driven high.

If instead of ANYRQST being held high jumper E170 to E171 is installed and E175 is connected for E183, the bus is surrendered according to Table 4-10.

In any mode of arbiter operation either OVERRIDE or PROC LOCK/ go active, the arbiter is prevented from surrendering the system bus to any other bus arbiter regardless of its priority.

PROC LOCK/ is generated by the 80186 Microprocessor. OVERRIDE is generated by the 74LS259 Program Latch located at U26.

Table 4-10. Requesting and Relinquishing the System Bus

S2/	S1/	S0/	CMD	SYSB/RESB (ON BD ADDR/)	MULTIBUS Requested (BREQ/)	MULTIBUS Surrendered
L	L	H	RD I/O	H	BREQ/ Low	—
L	H	L	WR I/O	H	BREQ/Low	—
L	H	H	HALT	H	—	MULTIBUS Surrendered
H	L	H	MEM RD	H	BREQ/ Low	
H	H	L	MEM WR	H	BREQ/ Low	
H	H	H	IDLE	H		MULTIBUS Surrendered
L	L	H	RD I/O	L	—	MULTIBUS Surrendered
L	H	L	WR I/O	L	—	MULTIBUS Surrendered
L	H	H	HALT	L		
H	L	H	MEM RD	L	—	MULTIBUS Surrendered
H	H	L	MEM WR	L	—	MULTIBUS Surrendered
H	H	H	IDLE	L	—	MULTIBUS Surrendered

4.3.7 SLAVE ADDRESS DECODE LOGIC

During a MULTIBUS interface access of on-board RAM the MULTIBUS interface master can address the iSBC 186/51S board as a slave RAM. The bus master first places the address on the MULTIBUS interface and then asserts MRDC/ or MWTC/. The slave address decode logic (sheet 5 of schematic 146976) is used to decode the MULTIBUS addresses for dual port RAM access. The slave address decode logic is made up of a 3625A-1 Address Translation PROM and six exclusive-OR gates located at U75 and U80.

The Exclusive-OR gates do a decode of the upper six address lines (ADR12 through ADR17). The second inputs to each of the Exclusive-OR gates are provided by a series of jumpers which select one 1M Byte page of 16 possible pages as shown below:

E180-E188	E150-E153	E158-E161	E157-E160	E151-E154	Megabyte Page Selected
X	-	-	-	-	OXXXXX(H)
X	-	-	-	X	1XXXXX(H)
X	-	-	X	-	2XXXXX(H)
X	-	-	X	X	3XXXXX(H)
X	-	X	-	-	4XXXXX(H)
X	-	X	-	X	5XXXXX(H)
X	-	X	X	-	6XXXXX(H)
X	-	X	X	X	7XXXXX(H)
X	X	-	-	-	8XXXXX(H)
X	X	-	-	X	9XXXXX(H)
X	X	-	X	-	AXXXXX(H)
X	X	-	X	X	BXXXXX(H)
X	X	X	-	-	CXXXXX(H)
X	X	X	-	X	DXXXXX(H)
X	X	X	X	-	EXXXXX(H)
X	X	X	X	X	FXXXXX(H)

X = Jumper Installed
- = Jumper Out

When the states of the six address bits match the jumpers installed, the slave address gate at U9 is enabled.

The address translation PROM at U82 performs two functions. First, it decodes the next three address bits ADRF/, ADR10/ and ADR11/ using the size and top address jumpers to determine if the MULTIBUS address is in the range of the dual port address mapping. If the MULTIBUS address is in range as determined by the jumpers the MULTIBUS addresses, ATRF/, ATR10/ and ATR11/, are translated as they map onto the appropriate dual port RAM address. Table 4-11 shows the PROM programming.

Table 4-11. Address Translation PROM U82 Programming

	INPUTS															
	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
000	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	00
010	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	00	0F	01
020	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	01	00	0F
030	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	00	0F	01	0F
040	0F	0F	0F	0F	0F	0F	0F	00	0F	0F	0F	0F	01	0F	0F	0F
050	0F	0F	0F	0F	0F	00	0F	01	0F	0F	0F	0F	0F	0F	0F	0F
060	0F	0F	0F	0F	0F	01	00	0F	0F	0F	0F	0F	0F	0F	0F	0F
070	0F	0F	0F	0F	00	0F	01	0F	0F	0F	0F	0F	0F	0F	0F	0F
080	0F	0F	0F	0F	0D	0D	0D	0D	0F	0F	0F	0F	0D	0D	0D	04
090	0F	0F	0F	0F	0D	0D	0D	0D	0F	0F	0F	0F	0D	04	0D	0D
0A0	0F	0F	0F	0F	0D	0D	0D	0D	0F	0F	0F	0F	0D	0D	04	0D
0B0	0F	0F	0F	0F	0D	0D	0D	0D	0F	0F	0F	0F	04	0D	0D	0D
0C0	0F	0F	0F	0F	0D	0D	0D	04	0F	0F	0F	0F	0D	0D	0D	0D
0D0	0F	0F	0F	0F	0D	04	0D	0D	0F	0F	0F	0F	0D	0D	0D	0D
0E0	0F	0F	0F	0F	0D	0D	04	0D	0F	0F	0F	0F	0D	0D	0D	0D
0F0	0F	0F	0F	0F	04	0D	0D	0D	0F	0F	0F	0F	0D	0D	0D	0D
100	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	00
110	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	00	0F	01
120	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	01	00	02
130	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	00	02	01	03
140	0F	0F	0F	0F	0F	0F	0F	00	0F	0F	0F	0F	01	03	02	0F
150	0F	0F	0F	0F	0F	00	0F	01	0F	0F	0F	0F	02	0F	03	0F
160	0F	0F	0F	0F	0F	01	00	02	0F	0F	0F	0F	03	0F	0F	0F
170	0F	0F	0F	0F	00	02	01	03	0F	0F	0F	0F	0F	0F	0F	0F

Table 4-11. Address Translation PROM U82 Programming (Cont'd.)

	INPUTS															
	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
180	0F	0F	0F	0F	0D	0D	0D	0D	0F	0F	0F	0F	0D	0D	0D	04
190	0F	0F	0F	0F	0D	0D	0D	0D	0F	0F	0F	0F	0D	04	0D	05
1A0	0F	0F	0F	0F	0D	0D	0D	0D	0F	0F	0F	0F	0D	05	04	0D
1B0	0F	0F	0F	0F	0D	0D	0D	0D	0F	0F	0F	0F	04	0D	05	0D
1C0	0F	0F	0F	0F	0D	0D	0D	04	0F	0F	0F	0F	05	0D	0D	0D
1D0	0F	0F	0F	0F	0D	04	0D	05	0F	0F	0F	0F	0D	0D	0D	0D
1E0	0F	0F	0F	0F	0D	05	04	0D	0F	0F	0F	0F	0D	0D	0D	0D
1F0	0F	0F	0F	0F	04	0D	05	0D	0F	0F	0F	0F	0D	0D	0D	0D
200	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	00
210	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	00	0F	01
220	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	01	00	02
230	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	00	02	01	03
240	0F	0F	0F	0F	0F	0F	0F	00	0F	0F	0F	0F	01	03	02	04
250	0F	0F	0F	0F	0F	00	0F	01	0F	0F	0F	0F	02	04	03	05
260	0F	0F	0F	0F	0F	01	00	02	0F	0F	0F	0F	03	05	04	0F
270	0F	0F	0F	0F	00	02	01	03	0F	0F	0F	0F	04	0F	05	0F
280	0F	0F	0F	0F	0D	0D	0D	0D	0F	0F	0F	0F	0D	0D	0D	04
290	0F	0F	0F	0F	0D	0D	0D	0D	0F	0F	0F	0F	0D	04	0D	05
2A0	0F	0F	0F	0F	0D	0D	0D	0D	0F	0F	0F	0F	0D	05	04	06
2B0	0F	0F	0F	0F	0D	0D	0D	0D	0F	0F	0F	0F	04	06	05	0D
2C0	0F	0F	0F	0F	0D	0D	0D	04	0F	0F	0F	0F	05	0D	06	0D
2D0	0F	0F	0F	0F	0D	04	0D	05	0F	0F	0F	0F	06	0D	0D	0D
2E0	0F	0F	0F	0F	0D	05	04	06	0F	0F	0F	0F	0D	0D	0D	0D
2F0	0F	0F	0F	0F	04	06	05	0D	0F	0F	0F	0F	0D	0D	0D	0D
300	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	00
310	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	00	0F	01
320	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	01	00	02
330	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	00	02	01	03
340	0F	0F	0F	0F	0F	0F	0F	00	0F	0F	0F	0F	01	03	02	04
350	0F	0F	0F	0F	0F	00	0F	01	0F	0F	0F	0F	02	04	03	05
360	0F	0F	0F	0F	0F	01	00	02	0F	0F	0F	0F	03	05	04	06
370	0F	0F	0F	0F	00	02	01	03	0F	0F	0F	0F	04	06	05	07
380	0F	0F	0F	0F	0D	0D	0D	0D	0F	0F	0F	0F	0D	0D	0D	04
390	0F	0F	0F	0F	0D	0D	0D	0D	0F	0F	0F	0F	0D	04	0D	05
3A0	0F	0F	0F	0F	0D	0D	0D	0D	0F	0F	0F	0F	0D	05	04	06
3B0	0F	0F	0F	0F	0D	0D	0D	0D	0F	0F	0F	0F	04	06	05	07
3C0	0F	0F	0F	0F	0D	0D	0D	04	0F	0F	0F	0F	05	07	06	0D
3D0	0F	0F	0F	0F	0D	04	0D	05	0F	0F	0F	0F	06	0D	07	0D
3E0	0F	0F	0F	0F	0D	05	04	06	0F	0F	0F	0F	07	0D	0D	0D
3F0	0F	0F	0F	0F	04	06	05	07	0F	0F	0F	0F	0D	0D	0D	0D

Values shown are in Hexadecimal

Second, assuming the MULTIBUS address is within the range of the dual port mapping, the slave address request gate, U9, generates SLAVE ADD REQUEST to the dual port control logic. SLAVE ADD REQUEST being active generates SLAVE RAM REQUEST active, since either MRDC/ or MWTC/ will also be active. MRDC/ or MWTC/ being active will generate either BUS RD CMD/ or BUS WT CMD/ and BUS CMD active to the dual port control logic.

4.3.8 DUAL PORT MEMORY AND DUAL PORT SELECT LOGIC

The dual port select logic consists of two PALs located at U37 and U56, three 74S175 quad D-type flip-flops, at U39 and a 74S74 flip-flop at U57.

PAL U56 generates the local access command to the dual port. PAL U37 generates the slave access commands to the dual port. Table 4-12 shows the programming for PAL U56 and Table 4-13 is the programming for PAL U37.

The state of ON BD DP REQ/ generated by PAL U56 (Table 4-12) is determined by three signals, address bits A12 and A13 and the 304EN/ signal. If the iSBC 304 Memory Expansion Board is installed on the iSBC 186/51S board, 304EN/ will be low and address bit A13 must go high and A12 low for an active ON BD DP REQ/. If the iSBC 304 board is not installed, 304EN/ will be high and address bits A12 and A13 low for an active ON BD DP REQ/. ON BD DP REQ/ does two things: 1) it blocks any slave dual port accesses and, 2) it is used in the ready logic PAL at U40. ON BD DP REQ/ can be prevented when T21 is inactive or the on-board processor requests an I/O operation instead of a memory operation (MEM/$\overline{IO}$ low) or EARLY CMD is inactive.

The LOCAL DP RD/ (Local Dual Port Read) and LOCAL DP WT/ (Local Dual Port Write) commands initiate either a read or write operation in the dual port memory. The states of these signals are determined by EARLY CMD and LS1/. LS1/ is the latched status 1 bit (S1/) from the on-board processor. LS1/ low causes a read command, LS1/ high, a write command.

The Dual Port Request output (DPRO at U56-15) is gated with MPR0/ (Memory Protect) from the MULTIBUS interface. MPR0/ inactive enables the gate. Equation 4 in Table 4-12 shows that DPRQ can be generated if slave mode is active

or inactive, providing all other signal states are as indicated in Table 4-12. When SLAVE MODE is active, SCE, the $\overline{Q}$ output of flip-flop U39 (sheet 6 of schematic 146976) will go low one 16M CLK later. Before that clock occurs, both SCE and SLAVE MODE will be high. The second term of equation 4 in Table 4-12 will generate DPRQ active causing DP ACCESS/ to to low. DPACCESS/ low enables the 8203A Dynamic RAM Controller at U64. DP ACCESS/ needs to remain low only until the read or write operation in the dual port RAM starts.

Table 4-12. Dual Port Control I PAL U56 Programming

1. ONBDDPREQ (L) = (A13(L) · A12(L) · A11(L) · MEMIO(H)
   · EARLY CMD(H) · 304EN(H) · T21(H))
   + (A13(L) · A12(L) · A11(L) · MEMIO(H)
   · EARLY CMD(H) · 304EN(L) · T21(H)
   + (A13(L) · A12(L) · A11(H) · MEMIO(H)
   · EARLYCMD(H) · 304EN(L) · T21(H))
2. LOCALDPRD (L) = EARLY CMD(H) · LSI(L) ·T21(H)
3. LOCALDPWT (L) = EARLY CMD(H) · LSI(H) ·T21(H)

NOTE

In the next equation SCE is the $\overline{Q}$ output at U39-11 and DPRQ is the PAL output at U56-15.

4. DPRQ(L) = (SCE(H) · T21(L)) + (SCE(H) · SLAVE MODE(H))
   + (SCE(H) · EARLY CMD(L)) + (SCE(H) · MEMIO(L))
   + (SCE(H) · A13(H)) + (SCE(H) · A12(H))
   + (SCE(H) · A11(H) · 304EN(H))

Table 4-12. Dual Port Control 1 PAL U56 Programming (Cont'd.)

5. ONBDCMD (L) = (SCE(H) · SLAVE MODE(L) · EARLY CMD(H) · A13(L)
· A12(L) · A11(L) · MEMIO(H))
+ (SCE(H) · SLAVEMODE(L) · EARLY CMD(H)
· A13(L) · A12(L) · A11(L) · MEMIO(H)
· 304EN(L))

6. ACAS(L) = CAS

7. DCAS(H) = ACAS

NOTE

ACAS is the output at U56-16. It is used internally in the PAL. Pin U56-16 cannot be used for any other purpose despite being shown as unconnected.

Table 4-13. Dual Port Control 2 PAL U37 Programming

NOTE

SRQ1 is the PAL output at U37-13.

1. SRQ1(L) = (SLAVE RAM REQUEST(L) · T21(H) · ONBDLOCK(H)
· SLAVE RAM REQUEST(L) · T21(H) · BREQ(L)

NOTE

SCE is output at U39-11.

Table 4-13. Dual Port Control 2 PAL U37 Programming (Cont'd.)

2. SLAVE CMD(L) = SLAVE MODE(H) · INHIBIT(L) · SLAVE RAM REQUEST(L) · SCE(L)

NOTE

SHOLD is the PAL output at U37-12. RHOFF is the PAL input at U37-3.

3. SHOLD(L) = RHOFF(H) + SLAVE RAM REQUEST(L) + XX3

NOTE

XACKEN is the PAL output at U37-18.

4. XACKEN(L) = (SLAVE RAM REQUEST(L) · DPXACK(L) · SLAVE MODE(H) · INHIBIT(L) · SCE(L) · FLAG XACK(L))

5. SSS(L) = SO(H) · SI(H)

6. XX3 = RHOFF(H) + SLAVE RAM REQUEST (L)

If slave mode is not active, SLAVE MODE will be low and SCE will be high. DPRQ can than be generated as shown in Table 4-12.

ON BD CMD/ is generated as shown in Equation 5 of Table 4-12. ON BD CMD/ is applied to the buffers located at U35 to enable the local dual port read or write commands to the 8203 Controller in the dual port RAM.

PAL U37 generates the slave access requests as shown in Table 4-13. SRQ1 (Slave Request 1), equation 1 of Table 4-13 shows that SRQ1 can be blocked by T21 inactive, ONBDLOCK active low or BREQ/ inactive. If SRQ1 is generated active low, the next 16 MHz CLOCK will clock it through the synchronizer flip-flop at U48. Since SLAVE ADD REQUEST will also be active, AND-gate U36-12 will be place a high at the input of dual port arbitration flip-flop U57. Another 16 MHZ CLK later SLAVE MODE/ will go low and SLAVE MODE will go high. SLAVE MODE high is returned to PAL U56 where it prevents ON BD CMD/ from being generated active. The dual port RAM array will be prevented from responding to any local dual port read or write command.

With SLAVE MODE high, SLAVE RAM REQ high, SCE low and INHIBIT low PAL U37 will generate SLAVE CMD/ (U37-19) active low, equation 2 of Table 4-13. SLAVE CMD/ is applied to the drivers at U52, sheet 7 of schematic 146976 and permits the BUS RD CMD/ or the BUS WT CMD/ to be read by the 8203 controller in the dual port RAM. BHEN/ enable is also enabled by SLAVE CMD/.

Slave mode will be terminated when the slave release flip-flop at U39 is allowed to change. The flip-flop will change when PAL U37 generates SHOLD (pin U37-12) low as shown in equation 3 of Table 4-13. One 16 MHz CLK after SHOLD goes low, AND-gate U77 generates a low clearing the dual port arbitration flip-flop U57 during SLAVE MODE/ high and SLAVE MODE low.

4.3.9 DUAL PORT RAM

The Dual Port RAM consists of a 16 2164 dynamic RAM array and an 8203 Dynamic RAM Controller device (U64). The dual port memory size is 128K Bytes, expandable to 256K Bytes with an optional iSBC 304 Memory Expansion MULTIMODULE.

The dual port RAM is always located at the bottom (the lowest local address) of the 80186 processor. The local address range of the dual port RAM is 0000(H) through 1FFFF(H), with the iSBC 304 MULTIMODULE installed the local address range becomes 0000(H) through 3FFFF(H). As seen from the MULTIBUS interface the address of the dual port RAM can be mapped anywhere in the 16M Byte address space. The amount of dual port RAM visible to the MULTIBUS can be one-fourth, one-half, three-fourths or all of the RAM. When less than all of the dual port RAMs visible to the MULTIBUS interface the visible portion is mapped to the upper portion of the local processors dual port address range.

The 8203 Dynamic RAM Controller provides multiplexed addresses, address strobes and refresh/access arbitration for the RAM array. The operation of the 8203 controller is configured at the factory before shipment and should not be changed. The memory refresh cycles are internally requested and internally generated by the 8203 device.

In response to chip select terms and an address the 8203 controller generates the row address strobe signal (RAS/), the column address strobe signal (CAS/) and the eight-bit cell address required to access the memory array during read, write and refresh operations.

The 8203 Controller will always be in one of the following states:

- o Idle
- o Write Cycle
- o Read Cycle
- o Refresh Cycle

In the idle state the controller monitors internal and external cycle requests and counts toward generation of an internal refresh cycle for the 2164 RAMs.

A write cycle is initialized when the WR/ input (pin U64-31) to the 8203 Controller is driven low. This input is driven low when either LOCAL DP WT/ and SLAVE CMD are driven low, or BUS WT CMD/ and DBDCMD are driven low (see section 4.3.6). During the write cycle, an address is input at AL0 through AL6 (row addresses) and AH0 through AH6 (column addresses) to generate the row and column addresses for the memory array. The 8203 controller generates the row and column address strobe signals RAS/ and CAS/, respectively, when the row and column address on the OUT0/ through OUT7/ are valid. Write enable (WE/) to the memory array is generated as a result of four signals WE/ from the 8203 controller AB0 from the 80186 processor and BHEN/ (byte high enable) or BHE/. WE1/ to the first eight RAMs (U67 through U74) will be active when WE/from the 8203 controller and AB0 are both low. WE2/ to the second group of eight RAMs (U87 through U94) goes low when WE/ from the 8203 controller, AB0 and BHEN/ (Byte High Enable) or OB BHEN are all low. WE2/ to the second group of eight RAM can also go active when WE/from the 8203 controller is low and AB0 is high.

With RAS/, CAS/, WE1/ and WE2/ signals generated the RAM array begins the data storage operation. When the storage operation is completed the 8203 Controller generates XACK/ (U64-29). As configured from the factory REFRQ is held at

ground allowing the 8203 Controller to control the refresh function internally. Stake pins E216 and E215 provide an external refresh request. This function is used for factory test purposes only.

The read cycle operation within the dynamic RAM controller is identical to that of the write cycle except that the RD/ input (U64-32) to the 8203 controller is driven low, LOCAL DP RD/ and DBD CMD/ going low, or BUS RD CMD/ and SLAVE CMD/ going low. The write enable signals (WE/, WE1/, and WE2/) are held inactive on the board. Figure 4-4 shows a typical dynamic RAM operation sequence.

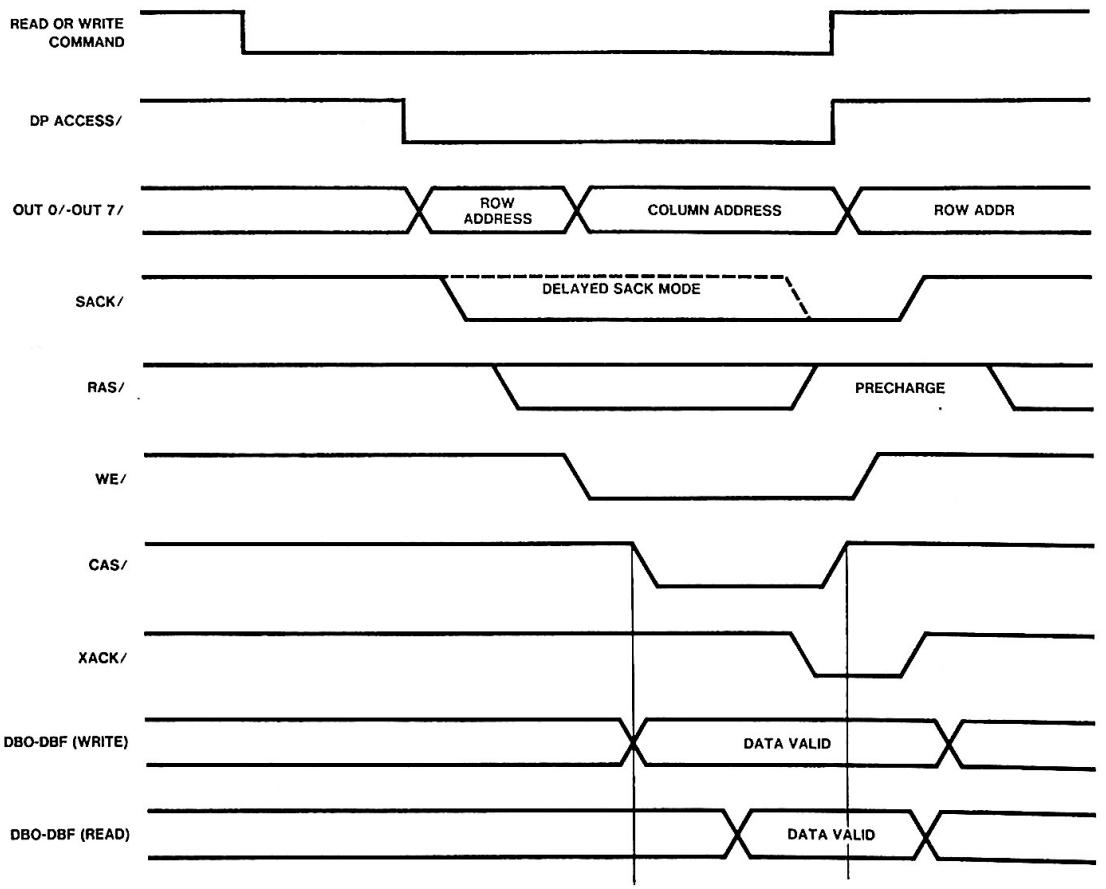


Figure 4-4. Typical Dynamic RAM Operation Sequence

4.3.10 LOCAL MEMORY CIRCUITS

The local memory circuits of the iSBC 186/51S are divided into two circuit groups, the local memory site (sheet 9 of schematic 146976) and the local memory select logic (sheet 8 of the schematic).

The local memory site has six 28-pin JEDEC connectors. The six connectors are configured as three pairs, providing a full 16-bit bus. The site can contain a mix of user supplied ROM, PROM, RAM, and iRAM. Memory device types can be mixed between pairs, but not within a pair.

The iSBC 186/51S is compatible with four sizes of memory devices 4, 8, 16, or 32K. The memory device addressing ranges depend on the size of the memory device installed. The address range for each size memory device is summarized below:

Sockets	4K Device	8K Device	16K Device	32K Device
U34, U51	FE000-FFFFF	FC000-FFFFF	F8000-FFFFF	F0000-FFFFF
80130	---	F8000-FBFFF	F0000-F7FFF	E0000-EFFFF
U33, U50	FA000-FBFFF	F4000-F7FFF	E8000-EFFFF	D0000-DFFFF
U32, U49	F8000-F9FFF	F0000-F3FFF	E0000-E7FFF	C0000-CFFFF

The address location of the local memory sockets are at the top of the 1M Byte address space of the 80186. The three socket pairs are designated 3 (U34, U51), 1 (U33, U50) and 0 (U32, U49). Socket pair 2 is the kernal memory in the 80130 device. This configuration allows local memory to exist on each side of the 80130 kernal memory. If 4K parts are used, the 80130 kernal cannot be accessed.

A stake pin matrix allows configuring the local memory site for all specified devices. The stake pin configurations for each type memory device is shown in Section 2 of this manual. In the "as shipped" configuration of the iSBC 186/51S board, iRAMs can be installed in the U32/U49 and U33/U50 socket pairs.

The stake pin matrix for each socket pair is an Intel standard matrix. The functions associated with each pin are as shown:

E91 V_{CC}	E92 (U38/U51),U94(To Site Pin 1
E95 Address Bit 15 (A10)	E96 PROM RDY
E99 To Site Pin 1	E100
E103 Address Bit 14 (AF)	—
E105 To Site Pin 27	E106 WE/ (Write Enable)
E109 V_{CC}	E110 To Site Pin 23
E113 V_{CC}	E114 Address Bit 11 (AC)
E117 To Site Pin 26	E118 Address Bit 13 (AE)

Jumpers shown installed are for the default condition. Stake pins shown are for the U34/U51 JEDEC pair. Stake pin connections for the two other pairs ((U33/U50) and (U32/U49)) are as shown:

U34/U51	U33/U50	U32/U49
E91	E93	E135
E92	E94	E136
E95	E97	E137
E96	E98	E138
E99	E101	E139
E100	E102	E140
E103	E104	E141
E105	E107	E142
E106	E108	E143
E109	E111	E144
E110	E112	E145
E113	E115	E146
E114	E116	E147
E117	E119	E148
E118	E120	E149

The local memory select logic consists of a PAL device at U59 and a 74S139 Decoder Multiplexer at U53. PAL programming is shown in Table 4-13. The PAL monitors the upper address lines and the MEM/$\overline{IO}$ line to decide if the local memory is being selected. Two PAL input lines, U59-17 and U59-18, select the size of the local memory sockets 4, 8, 16, or 32K. The connections between stake pins encodes these inputs as follows:

E199-E203	E203-E191	Size Selected
In	In	4K
In	Out	8K
Out	In	16K
Out	Out	32K

Table 4-14. Local Memory Chip Select Decode PAL U59 Programming

NOTE
RSZ0 is PAL input U59-17.
RSZ1 is PAL input U59-18.

1. PROMSEL(L) = (A13(H) · A12(H) · A11(H) · A10(H) · AF(H)
· RSZ1(L) · RSZ0(L) · MEM/$\overline{IO}$(H) · EARLY CMD(H))
+ (A13(H) · A12(H) · A11(H) · A10(H) · RSZ1(L)
· RSZ0(H) · MEM/$\overline{IO}$(H) · EARLY CMD(H))
+ (A13(L) · A12(H) · A11(H) · RSZ1(H) · RSZ0(L)
· MEM/$\overline{IO}$(H) · EARLY CMD(H))
+ (A13(H) · A12(H) · RSZ1(H) · RSZ0(H)
· MEM/$\overline{IO}$(H) · EARLY CMD(H))

NOTE
OBM is PAL output U59-15

2. OBM(L) = (A13(H) · A12(H) · A11(H) · A10(H) · AF(H)
· RSZ1(L) · RSZ0(L) · MEM/$\overline{IO}$(H))
+ (A13(H) · A12(H) · A11(H) · A10(H) · RSZ1(L)
· RSZ0(H) · MEM/$\overline{IO}$(H))
+ (A13(H) · A12(H) · A11(H) · RSZ1(H) · RSZ0(L)
· MEM/$\overline{IO}$(H))
+ (A13(H) · A12(H) · RSZ1(H) · RSZ0(H) · MEM/$\overline{IO}$(H))
+ (A13(L) · A12(L) · A11(L) · 304EN(H) · MEM/$\overline{IO}$(H))
+ (A13(L) · A12(L) · A11(L) · 304EN(L) · MEM/$\overline{IO}$(H))
+ (A13(L) · A12(L) · A11(H) · 304EN(L) · MEM/$\overline{IO}$(H))

NOTE
RSL1 is PAL output U59-12.
RSL0 is PAL output U59-13.

Table 4-14. Local Memory Chip Select Decode PAL U59 Programming (Cont'd.)

3. RSL1(L) = (MEM/$\overline{IO}$ (H) · A13(H) · A12(H) · A11(H) · A10(H)
· AF(H) · RSZ1(L) · RSZ0(L) · AE(L) · EARLY CMD(H)
· ALE(L)) + (MEM/$\overline{IO}$ (H) · A13(H) · A12(H)
· A11(H) · A10(H) · RSZ1(L) · RSZ0(L) · AF(L) · ALE(L)
· EARLY CMD(H)) + (MEM/$\overline{IO}$ (H) · A13(H) · A12(H)
· A11(H) · RSZ1(H) · RSZ0(L) · A10(L) · ALE(L)
· EARLY CMD(H)) + (MEM/$\overline{IO}$ (H) · A13(H) · A12(H)
· RSZ1(H) · RSZ0(H) · A11(L) · EARLY CMD(H) · ALE(L))

4. RSL0(L) = (RSZ1(L) · RSZ0(L) · AD(H)) + (RSZ1(L) · RSZ0(H)
· AE(H)) + (RSZ1(H) · RSZ0(L) · AF(H)) + (RSZ1(H)
· RSZ0(H) · A10(H))

5. KERNAL CS(L) = (A13(H) · A12(H) · A11(H) · A10(H) · AF(H) · AE(H)
· AD(L) · RSZ1(L) · RSZ0(L) · MEM/$\overline{IO}$ (H))
+ (A13(H) · A12(H) · A11(H) · A10(H) · AF(H) · AE(L)
· RSZ1(L) · RSZ0(H) · MEM/$\overline{IO}$ (H)) + (A13(H)
· A12(H) · A11(H) · A10(H) · AF(L) · RSZ1(H)
· RSZ0(L) · MEM/$\overline{IO}$ (H)) + (A13(H) · A12(H)
· A11(H) · A10(L) · RSZ1(H) · RSZ0(H)
· MEM/$\overline{IO}$ (H))

The upper address lines A0 through A13 are always logical "1" for local memory selection and MEM/$\overline{IO}$ must be in the memory state (high). In addition to the address and MEM/$\overline{IO}$ inputs to the PAL, the PAL output at U59-12 (RSL1) is gated internally on the PAL with ALE and EARLY CMD and with T21 between the PAL and the 74S139 decoder. This internal and external gating is required to provide a clean chip select signal, required for the iRAMs which may be used in the local memory. Only the PROM0 and PROM1 chip select signals are so gated. The ALE input prevents PROM0 Low CS/, PROM0 High CS/, PROM1 Low CS/ and PROM1 High CS/ from being generated early in the cycle. T21 inactive continues the blocking of PROM0 and PROM1 chip selects until it goes active. At the start of T21 both chip selects can be enabled. The chip selects are removed when EARLY CMD goes inactive at the end of COMMAND, flip-flop U79 (sheet 6 of schematic 146976). T21 is gated external to the PAL to ensure enough chip select to the COMMAND time for the byte wide devices. The two lines applied to the decoder are a function of the socket address size inputs.

The A0 and BHE/ signals are used to enable the two halves of the 74S139 decoder. Either or both halves can be enabled, allowing byte as well as word accesses of the local memory.

Table 4-15 shows the decoding done by the 74S139 decoder.

4.3.11 8274 SERIAL CHANNEL CIRCUITS

The serial interface circuit of the iSBC 186/51S board are shown on sheets 8 and 11 of schematic diagram 146976 in Section 5 of this manual. The primary device in the circuit is a 8274 Multi-Protocol Serial Controller (MPSC) located at U2. The MPSC to microprocessor system interface can be configured in different ways. The interrupt driven or direct memory access modes are used in the iSBC 186/51S configuration.

The interrupt driven operation is accomplished via the interrupt controller in the 80130A device. When the MPSC requires service it generates 8274 INT active to the 80130A processor. The 80130A processor, through the PAL at U30, returns 8274 INTA/, an interrupt acknowledge signal. The MPSC responds to an interrupt acknowledge sequence by placing a call instruction and interrupt vector on the data bus.

Table 4-15. Local Memory Decoder U53 Truth Table

INPUTS					PROM 1 Low CS	PROM 0 Low CS	PROM 3 Low CS	PROM 1 High CS	PROM 0 High CS	PROM 3 High CS
A0	BHE/	T21	RSL1 U59-12	RSL0 U59-13						
L	H	H	H	L	H	H	H	H	H	H
L	H	H	H	H	L	H	H	H	H	H
L	H	H	L	L	H	L	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H
H	L	H	H	L	H	H	H	H	H	H
H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	L	H
H	L	H	L	H	H	H	H	H	H	L
L	L	H	H	L	H	H	H	H	H	H
L	L	H	H	H	L	H	H	L	H	H
L	L	H	H	L	H	L	H	H	L	H
L	L	H	L	H	H	H	L	H	H	L

The MPSC can be programmed to cause an interrupt for 14 different conditions in each channel. These 14 conditions are all directed to cause three types of interrupts; receive interrupts, transmit interrupts and external status interrupts.

The MPSC is programmed to utilize up to four DMA channels, Transmit Channel A (TXDRQA), Receive Channel A (RXDRQA), Transmit Channel B (TXDRQB) and Receive Channel B (RXDRQB). Each DMA channel has its own DMA request line.

The MPSC is selected by PAL U41 in the I/O select logic. The A0 and A1 inputs to the MPSC are two address bits which select either Channel A or Channel B and selects either data or command information. Selection is as shown below:

MPSC Input	Address Bit	Function
A0	A1	When low A0(A1) selects Channel A. When high Channel B is selected. Channel selection is for both data and commands.
A1	A2	When low A1(A2) indicates data, when high commands are indicated.

In the iSBC 186/51S application the MPSC is operated in the asynchronous mode. In the asynchronous mode the MPSC must be initialized with the following information: character length (WR3; D7, D6 and WR5; D6, D5), clock rate (WR4; D7, D6), number of stop bits (WR4; D3, D2), odd, even or no parity (WR4; D1, D0), interrupt mode (WR1, WR2), and receiver (WR3; D0) or transmitter (WR5; D3) enable. When loading these parameters into the MPSC, WR4 information must be written before the WR1, WR3, WR5 parameters/commands. See the mode register set up that follows:

	D7	D6	D5	D4	D3	D2	D1	D0
WR3	00 Rx 5 b/char 01 Rx 7 b/char 10 Rx 6 b/char 11 Rx 8 b/char		AUTO ENABLES	0	0	0	0	Rx Enable
WR4	00 X1 Clock 01 X16 Clock 10 X32 Clock 11 X64 Clock		0	0	00 Enable Sync Modes 01 1 Stop Bit 10 1 1/2 Stop Bits 11 2 Stop Bits		EVEN/ ODD PARITY	Parity Enable
WR5	DTR	00 Tx 5 b/char 01 Tx 7 b/char 10 Tx 6 b/char 11 Tx 8 b/char		SEND BREAK	Tx ENABLE	0	RTS	0

For transmission via a modem or RS232C interface, the Request To Send bit (RTS) (WR5; D1) and Data Terminal Ready bit (DTR) (WR5; D7) must be set along with the Transmit Enable bit (WR5; D3). Setting the Auto Enables bit (WR3; D5) allows the programmer to send the first character of the message without waiting for a clear to send (CTS).

Both the Framing Error and Receive Overrun Error flags are latched and cause an interrupt, i.e., if status affects vector (WR1B; D2) is selected, the interrupt vector indicates a special Receive condition.

If the External/Status Interrupt bit (WR1; D0) is enabled, Break Detect (RR0; D7) and Carrier Detect (RR0; D3) will cause an interrupt. Reset External/Status Interrupts (WR0; D5, D4, D3) will clear Break Detect and Carrier Detect bits if they are set.

A status read after a data read will include error status for the next word in the buffer. If the Interrupt on First Character (WR1; D4, D3) is selected, then data and error status are held until an Error Reset command (WR0; D5, D4, D3) is given.

If the Interrupt on Every Character Mode bit (WR1; D4, D3) is selected, the interrupt vector is different if there is an error status in RR1. When the character

is read, the error status bit is set and the Special Receive Condition vector is returned if Status Affects vector (WR1B; D2) is selected.

In a polled environment, the Receive Character Available bit (RR0; D0) must be monitored so that the CPU can determine when data is available. The bit is reset automatically when the data is read.

The transmit function begins when the Transmit Enable bit (WR5; D3) is set. The MPSC automatically adds the start bit, the programmed parity bit (odd, even or no parity) and the programmed number of stop bits (1, 1.5 or 2 bits) to the data character being transmitted.

The Serial data is shifted out from the Transmit Data (TxD) output on the falling edge of the Transmit Clock (TxC) input, at a rate programmable to 1, 1/16, 1/32nd, or 1/64th of the clock rate supplied to the TxC input.

The TxD output is held high when the transmitter has no data to send, unless, under program control, the Send Break (WR5; D4) command is issued to hold the TxD low.

If the External/STATUS Interrupt bit (WR1; D0) is set, the status of CD, CTS and SYNDET are monitored, and, if any changes occur for a period of time greater than the minimum specified pulse width, an interrupt is generated. CTS is usually monitored using this interrupt feature.

If the Auto Enables (WR; D5) option is selected the programmer need not wait for the CTS before sending the first character. The MPSC will automatically wait for the CTS pin to go active before the transmission begins.

The Transmit Buffer Empty bit (RR0; D2) is set by the MPSC when the data byte from the buffer is loaded in the transmit shift register. The data is written to the MPSC only when the TX buffer becomes empty to prevent overwriting.

The receive function begins when the Receive Enable bit (WR3; D0) is set. If the Auto Enables (WR3; D5) option is selected, then Carrier Detect (CD) must also be low. A valid start bit is detected if a low persists for a least 1/2 bit time on the Receive Data (RxD) inputs.

The data is sampled at mid-bit time, on the rising edge of RxC, until the entire character is assembled. The receiver inserts 1's when a character is less than 8 bits. If parity (WR4; D1, D0) is enabled and the character is less than 8 bits the parity bit is not stripped from the character.

The receiver also stores error status for each of the 3 data characters in the data buffer. When a parity error is detected, the parity error flag (RR1; D4) is set and remains set until it is reset by the Error Reset command (WR0; D5, D4, D3).

When a character is assembled without a stop bit being detected, the Framing Error bit (RR1; D6) is set. The detection of a Framing Error adds an additional 1/2 bit time to the character time so the Framing Error is not interpreted as a new start bit.

If the CPU fails to read a data character while more than three characters have been received, the Receive Overrun bit (RR1; D5) is set. Only the overwritten character is flagged with the Receive Overrun bit. When this occurs, the fourth character assembled replaces the third character in the receive buffers. The Receive Overrun bit (RR1; D5) is reset by the Error Reset command (WR0; D5, D4, D3).

The A Channel of the 8274 can be configured for RS232C/DCE, RS232C DTE or for RS422A/449 operation. Figure 4-5 shows the signal paths for each of these configurations.

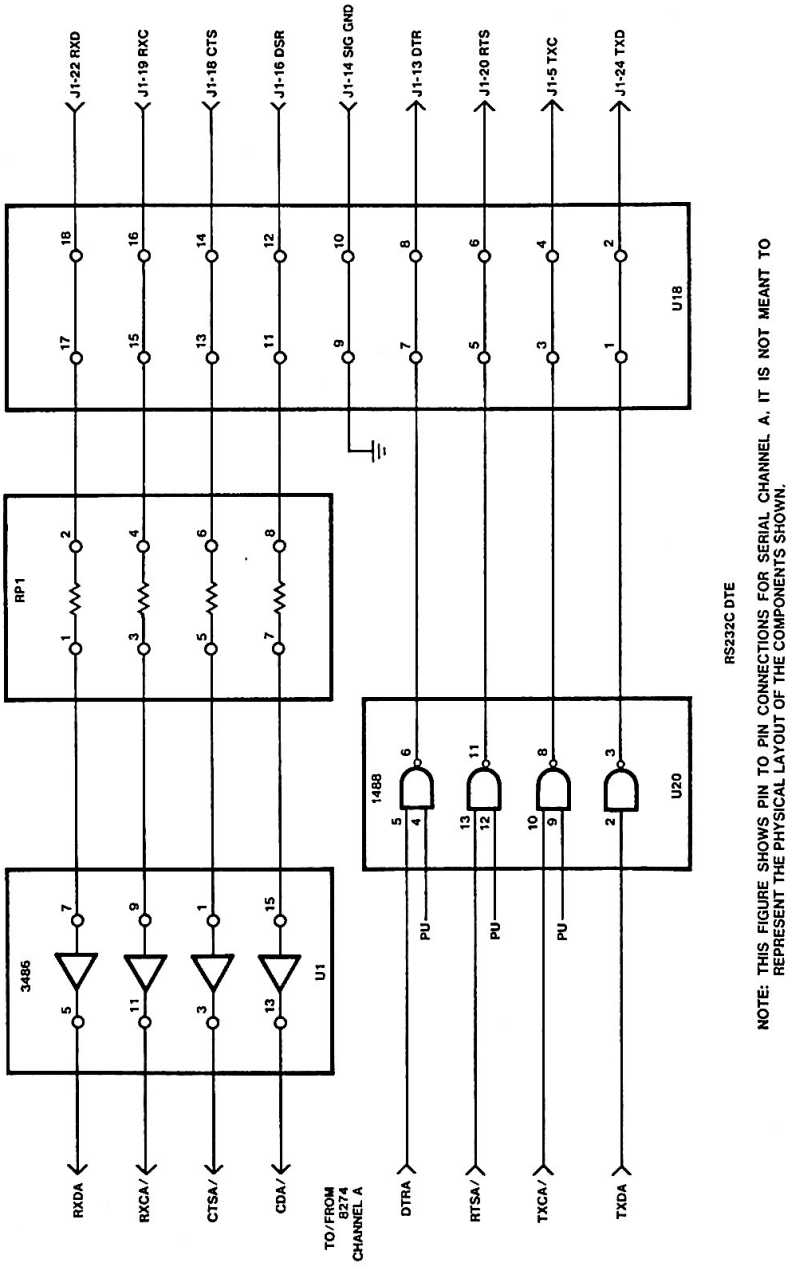


Figure 4-5. Serial Channel A Configuration (Sheet 1 of 3)

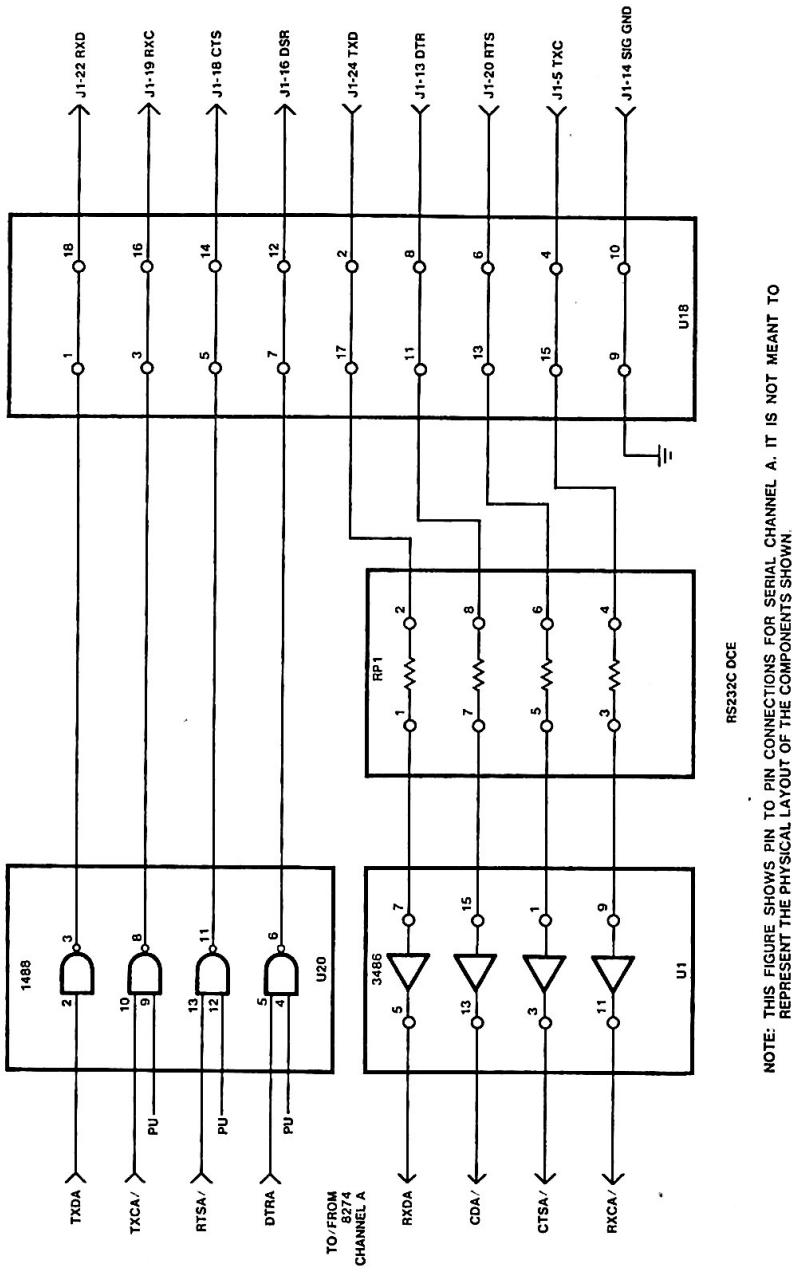
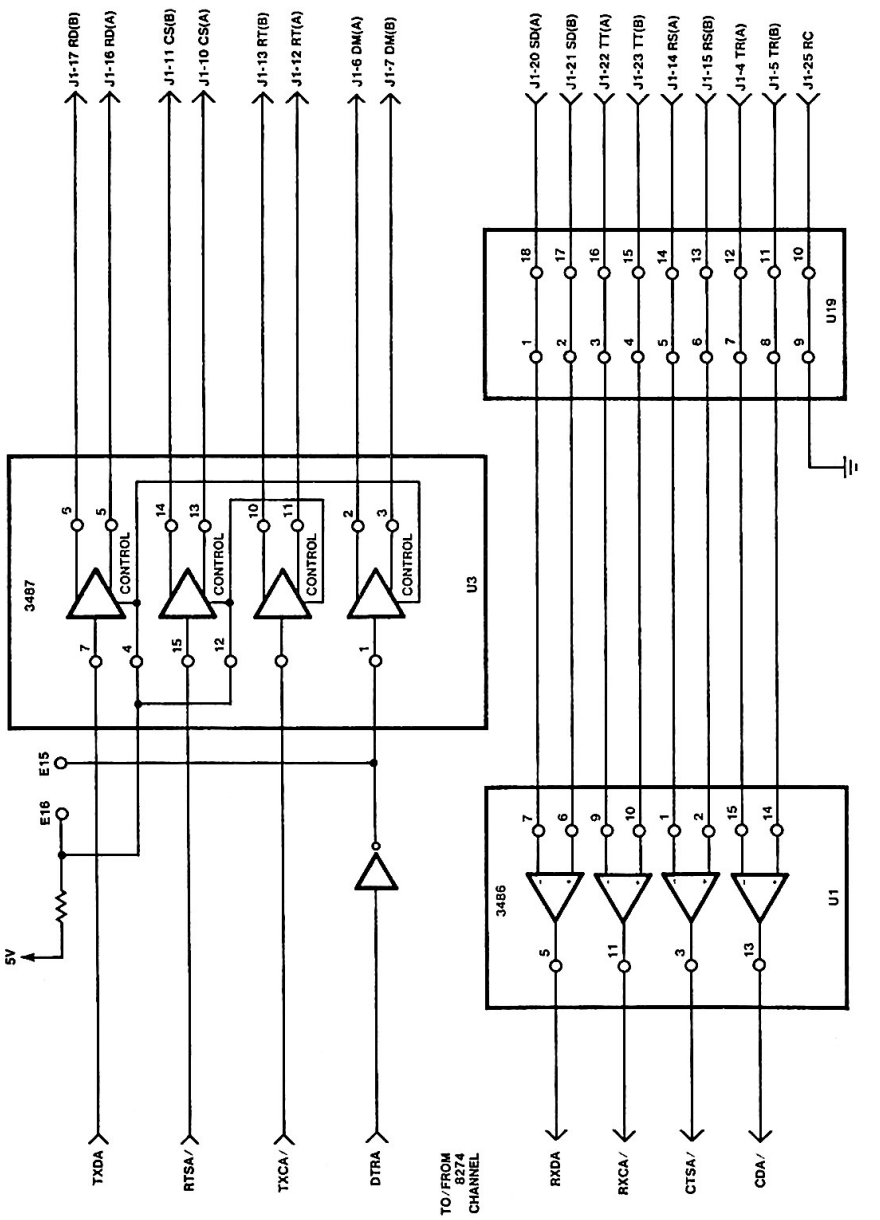


Figure 4-5. Serial Channel A Configuration (Sheet 2 of 3)



NOTE: THIS FIGURE SHOWS PIN TO PIN CONNECTIONS FOR SERIAL CHANNEL A. IT IS NOT MEANT TO REPRESENT THE PHYSICAL LAYOUT OF THE COMPONENTS SHOWN.

Figure 4-5. Serial Channel A Configuration (Sheet 3 of 3)

4.3.12 DEDICATED PARALLEL I/O CIRCUITS

A 74LS259 8-bit Addressable Latch located at U26 is used to create seven dedicated output lines. Four data inputs D8, D9, DA and DB are used for the data so either a word I/O write or an 8-bit I/O write to an odd address is required, with an 8-bit write recommended. The latch can be operated in four modes, as summarized in Table 4-16.

Table 4-16. Address Latch Modes

RESET/	LATCH CS/ · IOWC/	LATCHED MODES
H	L	**Addressable Latch Mode** – In the addressable-latch mode data at the data-in terminal, DB is written into the addressed latch. The addressed latch is determined by D8, D9 and D8 (see Table 4-17). The addressed latch will follow the data input with all unaddressed latches remaining in their previous states.
H	H	**Memory Mode** – In the memory mode all latches remain in their previous states and are unaffected by the data or address inputs
L	L	**Eight Line Demultiplexer Mode** – In this mode the addressed output will follow the level of the D input with all other outputs remaining low.
L	H	**Clear Mode** – All outputs are low and unaffected by the data inputs.

The data on the data bus gets strobed into the latch with the rising (trailing edge) of LATCH CS/ gated with IOWC/.

Table 4-17. Addressed Latches

DA	D9	D8	Latched Addresses
L	L	L	Latch 0 – LOOPBACK ESI/
L	L	H	Latch 1 – Unused
L	H	L	Latch 2 – NMI EN
L	H	H	Latch 3 – OVERRIDE
H	L	L	Latch 4 – NVEM
H	H	L	Latch 5 – MB INT
H	H	L	Latch 6 – DS3 input (User Determined)
H	H	H	Latch 7 – DS2 input (User Determined)

There are also four general purpose inputs to the processor which are user configured and determined by jumpers E133-E134, E128-E124, E123-E122 and E126-E129. Without the jumpers each level is a high level bit to the processor. By installing one or more jumpers a configuration code can be setup. For instance, if two sets of software existed on the iSBC 186/51S, a jumper or jumper combination could be used to tell the processor which software to run.

It is also possible to inform the processor of several other bits of information. This can be done by jumpering the outputs of latch U7 through the 74LS244 drivers at U35 to the processor. The jumpers and information they make available are summarized below:

Jumper	Indication
E127 to E126	A timeout has occurred (Bit 3).
E121 to E122	A timeout has occurred on the MULTIBUS (Bit 2).
E125 to E124	A software reset has occurred.
E132 to E133	A iSBC 304 Memory Expansion Board is installed. This input does not go through latch U7.

To read these inputs the processor does a byte I/O read of the 74LS244 driver at U35. I/O writes to this address are not performed to avoid bus contention.

4.3.13 FLAG BYTE CIRCUITS

The flag byte circuit consists of two PAL devices located at U83 and U11. The PAL at U83 is used as a MULTIBUS address decoder as shown in Table 4-18. If the iSBC 186/51S board is being used for 16-bit transfers, the jumper between E213 amd E209 is installed. If the board is being used for 8-bit transfers, the jumper is between E209 and E205. Jumper pairs E210-E206, E211-E207 and E212-E208 determine the flag byte address that will cause a PAL output at either U83-15 or U83-16. The flag byte addresses available are summarized below:

E210 to E206	E211 to E207	E212 to E208	16-Bit Address Selected	8-Bit Address Selected
Installed	Installed	Installed	08A4 (H)	A4 (H)
Installed	Installed	-	08A5 (H)	A5 (H)
Installed	-	Installed	08A6 (H)	A6 (H)
Installed	-	-	08A7 (H)	A7 (H)
-	Installed	Installed	09A4 (H)	A4 (H)
-	Installed	-	09A5 (H)	A5 (H)
-	-	Installed	09A6 (H)	A6 (H)
-	-	-	09A7 (H)	A7 (H)

The flag byte has two interrupts FLAG INT and BUS FLAG INT. FLAG INT is applied to the 80130A on-board interrupt controller (sheet 3 of schematic 146976) through jumper E51 to E55. BUS FLAG INT is brought out to stake pin E176 for connection to the MULTIBUS interface. FLAG INT is set by a MULTIBUS I/O write IOWC(L) low, first term of equation 2 in Table 4-19, and reset by an on-board write IOWT(L), fourth term of equation 2.

Table 4-18. Flag Byte Address Decode PAL U83 Programming

	FS0	FS1	FS2	ADR0	ADR1	ADR2	ADR3	ADR7	ADR8	ADR9	ADRA	ADRB	ADRC	ADRD	ADRE	ADRF
16BSEL = (L)	L	L	L	H	H	L	H	L	H	H	H	L	H	H	H	H
+	H	L	L	L	H	L	H	L	H	H	H	L	H	H	H	H
+	L	H	L	H	L	L	H	L	H	H	H	L	H	H	H	H
+	H	H	L	L	L	L	H	L	H	H	H	L	H	H	H	H
+	L	L	H	H	H	L	H	L	L	H	H	L	H	H	H	H
+	H	L	H	L	H	L	H	L	L	H	H	L	H	H	H	H
+	L	H	H	H	L	L	H	L	L	H	H	L	H	H	H	H
+	H	H	H	L	L	L	H	L	L	H	H	L	H	H	H	H
8BSEL = (L)	L	L	-	H	H	L	H	L	-	-	-	-	-	-	-	-
+	H	L	-	L	H	L	H	L	-	-	-	-	-	-	-	-
+	L	H	-	H	L	L	H	L	-	-	-	-	-	-	-	-
+	H	H	-	L	L	L	H	L	-	-	-	-	-	-	-	-

NOTES: L = Low Level State

H = High Level State

- = Not Applicable

16BSEL is PAL Output U83-16 (E213 connected to E209)

8BSEL is PAL Output U83-15 (E205 connected to E209)

FS0 is PAL Input U83-18

FS1 is PAL Input U83-17

FS2 is PAL Input U83-19

FLAG RES/ (Flag Reset) is activated by a MULTIBUS I/O Write (IOWC low), equation 3 of Table 4-19. When the U11-14 output of the PAL goes low it triggers the 74LS123 One-Shot Multivibrator at U13 which generates FLAG RES/ to the 80186 microprocessor. The MULTIBUS XACK signal is held up until the end of the reset pulse.

The states of two data bits to PAL U11 represent the flag byte signaling codes DAT0/ and DAT1/ are from the MULTIBUS interface and D0 and D1 are supplied by the on-board processor. The actions caused by the status codes and their source are shown below. Writing any other codes then those shown below will cause indeterminate action by the flag byte circuitry.

Data Written	Source	Action
04	On-Board Processor	Clear interrupt to on-board processor, FLAG INT inactive.
04	MULTIBUS Interface	Clear interrupt to MULTIBUS, BUS FLAG INT inactive.
02	On-Board Processor	Set interrupt to on-board processor, FLAG INT active.
02	MULTIBUS Interrupt	Set interrupt to MULTIBUS Interface, BUS FLAG INT active.
01	On-Board Processor	Clear interrupt to MULTIBUS.
01	MULTIBUS Interface	FLAG RES/ active.

Table 4-19. Flag Byte Logic PAL U11 Programming

NOTE

FLAG RES is PAL output U11-14.
FLAG INT is PAL output U11-15.
MB FLAG SEL is PAL output U83-16 or U83-15.

1. BUS FLAG INT (L) = (BUS FLAG INT(L) · D1(L))
+ (BUS FLAG INT(L) · D0(H))
+ (BUS FLAG INT(L) · IOWT(H))
+ (BUS FLAG INT(L) · FLAG CS(H)) + (RESET(L))
+ (DAT1(H) · DAT0(H) · IOWC(L) · ADR6(H)
· ADR5(L) · ADR4(H) · MB FLAG SEL(L))
+ (D1(L) · D0(H) · IOWT(L) · FLAGCS(L))

2. FLAG INT(L) = (DAT1(L) · DAT0(H) · IOWC(L) · ADR6(H) · ADR5(L)
· ADR4(H) · MBFLAGSEL(L) · RESET(H))
+ (FLAG INT(L) · D1(H) · RESET(H))
+ (FLAG INT(L) · D0(H) · RESET(H))
+ (FLAG INT(L) · IOWT(H) · RESET(H))
+ (FLAG INT(L) · FLAG CS(H) · RESET(H))

3. FLAG RES(L) = (DAT1(H) · DAT0(L) · IOWC(L) · ADR6(H) · ADR5(L)
· ADR4(H) · MBFLAGSEL(L))

4. FLAG XACK(L) = (DAT1(L) · DAT0(H) · IOWC(L) · ADR6(H)
· ADR5(L) · ADR4(H) · MBFLAGSEL(L) · FLAGINT(L))
+ (DAT1(H) · DAT0(H) · IOWC(L) · ADR6(H) · ADR5(L)
· ADR4(H) · MBFLAGSEL(L) · BUSFLAGINT(L))
+ (DAT1(H) · DAT0(L) · IOWC(L) · ADR6(H) · ADR5(L)
· ADR4(H)) · MBFLAGSEL(L) · FLAGRES (L))

4.4 Operation

Paragraphs 4.4.1 through 4.4.6 describe the various operating cycles of the iSBC 186/51S board.

4.4.1 TYPICAL READ CYCLE

A typical read cycle begins with the on-board processor, the 80186 or the 82586 asserting status (S0/ and S1/) followed by an address on the AD bus. The status bits are applied to Bus Controllers U25 and U81 (sheet 4 of schematic 146976). The status bits are coded as follows:

S0/	S1/	S2/	8288 Command
L	L	L	INTA/ (Not Used)
L	L	H	IORC/
L	H	L	IOWC/, AIOWC/
L	H	H	None
H	L	L	MRDC/
H	L	H	MRDC/
H	H	L	MWTC/, AMWC/
H	H	H	None

Address bits AD to A13 determine if the current cycle references the local memory, the dual port RAM or the MULTIBUS interface. Address bits AD through AD13 through PAL U59 (sheet 8 of 146976) generate the required chip select signals if the current cycle references the local memory. If the cycle references the dual port RAM, PAL U55 generates the appropriate local dual port commands. If the proper dual port commands are not generated by the on-board processor bits, the cycle references the MULTIBUS interface.

On-board transfers are either 8- or 16-bits as determined by the states of A0 and BHE/. In the case of a local memory transfer, A0 and BHE/ each enable one-half of the chip select decoder at U53. BHE/ active low enables the PROM1 HIGH CS/,

PROM0 HIGH CS/ and PROM3 HIGH CS/ signals, in 8-bit transfer on AD8 through ADF. A0 low enables the PROM1 LOW CS/, PROM0 LOW CS/ and PROM3 LOW CS/ signals, and 8-bit transfer. If both A0 and BHE/ are low, both PROM HIGH and LOW CS signals are enabled, a 16-bit transfer on lines AD0 through ADF occurs.

For either on-board dual port RAM data transfer or MULTIBUS data transfers, the 8- or 16-bit transfer modes are determined in the dual port array logic, sheet 7 of schematic 146976. For read cycles BLT U63 and the MULTIBUS SWAP signal determine the transfer mode. For write cycles AND-gates U22 and U66 using AB0, BHEN/ and WE/ from the 8203 Dynamic RAM Controller determine the data transfer mode. BHEN/ low transfers data on the high bit AD8 through ADF. AB0/ low transfers data on the low bit AD0 through AD7. AB0 and BHEN/ both low provide a 16-bit data transfer.

For a local memory read bus controller U25 after assertion of the status lines generates ALE to latch the address at latch U48. ALE is also applied to PROM Control PAL U38 where it generates T22 and T22/. When ALE is high, T22 is high, when ALE is low T22 is low (see Table 4-20). One buffered clock pulse (BUFF CLK) after ALE goes high T22 goes high enabling the command lines of bus controller U27 generating MEM RD/ to the local memory (sheet 9 of schematic 146876). MEM RD/ is ANDed with PROM SEL/, generated by PAL U59 (see Table 4-14) and initiates a read operation in the local memory.

During the on-board read operation ON BD ADDR/ is active disabling the command lines of bus controller U81.

MEM RD/ remains active until READY is generated by PAL U40 and sensed by the on-board processor, the 80186, or the 82586 LCC.

4.4.2 MEMORY WRITE CYCLE

A memory write cycle is identical to a memory read cycle except MEM WT/ is generated instead of MEM RD/ by bus controller U25. The MEM WT/ command (just as the MEM RD/ command) remains active until READY is sensed by the on-board processor.

Table 4-20. PROM Control PAL U38 Programming

1.	PCLK(H)	= PCLK(L)
2.	T22(L)	= ALE(H)
3.	T22I(L)	= ALE(L)

NOTE
HALTCLK is PAL output U38-17.

4.	HALTCLK(L)	= MEM/$\overline{IO}$(L) · LS1(L) · LS0(L)
5.	ON BD IO(L)	= PCS1(L) + (MEM/$\overline{IO}$(L) · LS1(L) · LS0(L)) + (ADRQ(L) · MEM/$\overline{IO}$(L))

NOTE
ABR0 is ADR0 buffered by U55.

6.	MULTIBUS SWAP(L)	= (ABR0(L) · BHEN(H) · SLAVE MODE(H)) + (ABR0(L) · BHEN(H) · BUS AEN(L))

4.4.3 TYPICAL INTERRUPT CYCLE

A typical interrupt cycle is one in which the 80130A device generates the interrupt vector.

The interrupt cycle is initiated when one of the interrupt lines to the 80130A device is asserted. In response to one of these interrupt requests (IR0 through IR7) going active the 80130A device raises INT0 to the 80186 processor. When the 80186 processor completes its current cycle, it drives its status lines (S0/, S1/ and S2/) to indicate an interrupt status. Those status bits are monitored by both the 80130A device and the 8288 Bus Controller, located at U25. In response to the status bits, the 8288 generates ALE latching the address A8, A9 and AA generated by the 80130A device. In this case the address has no significance.

When Ready Logic PAL U40 generates READY the 80186 processor starts another cycle, driving interrupt status but floating the AD bus. The 80130A device monitors the status lines from the 80186 processor and recognizes them as the second interrupt. The 80130A device then proceeds to drive the cascade address bits AD8, AD9 and ADA. The cascade address, however, is not decoded by PAL U30. During T3 the 80130A device puts the interrupt vector on the lower half of the AD bus (AD0 through AD7) which is read by the 80186 processor at the end of the cycle.

With the receipt of the 8-bit vector supplied by the 80130A device, the 80186 processor performs the remainder of the interrupt sequence as described in the 80186 data sheet.

4.4.4 8274 VECTORED INTERRUPT CYCLE

The 8274 Multi-Protocol Serial Controller can generate the interrupt vector if so determined by the cascade address decode PAL located at U30.

This kind of interrupt is initiated when one of the interrupt lines to the 80130A device is asserted. In response the 80130A device raises INT0 to the 80186 processor. When the 80186 processor completes its current cycle, it drives its status lines to indicate an interrupt status. These status bits are monitored by both the 80130A device and the 8288 Bus Controller, located at U25. In response to the status bits, the 8288 generates ALE which latches the cascade address bits A8, A9 and AA provided by the 80130A device. If the states of the address bits match the 8274 address, AA low, A9 high and A8 high, PAL U30 activate the Q3 output, interrupt wait. An active interrupt wait signal is required because more than two wait states are required to meet the timing requirements of the 8274 Controller. The 8274 INTA/ signal is then driven active for two clock cycles. This is the first interrupt cycle to the 8274 controller. The 8274 INTA/ signal is then made inactive for three clock periods. After the three clock periods the 8274 INTA/ signal is again driven active, for three clock cycles, the second interrupt cycle to the 8274 Controller.

The interrupt wait signal is removed at the start of the second 8274 INTA/ activation. The three clock cycles that the second 8274 INTA lasts allows the 8274 Controller to put its vector on the bus.

Table 4-21 shows programming for PAL U30 and Table 4-22 shows the state machine.

Table 4-21. Cascade Address PAL U30 Programming

NOTE

Q0 is PAL output U30-17
Q1 is PAL output U30-16
Q2 is PAL output U30-15
Q3 is PAL output U30-14
74ADDR is PAL output U30-19

1. Q3(L) = (Q3(L) · Q2(H) · Q1(H) · Q0(L) · ALE(L))
+ (Q3(H) · Q2(H) · Q1(H) · Q0(L) · ALE(L)
· 74ADDR(H))
+ (Q3(H) · Q2(H) · Q1(H) · Q0(L) · ALE(L)
· 74ADDR(L) · LIR(H))
+ (Q3(H) · Q2(L) · Q1(H) · Q0(L) · ALE(L)
· 74ADDR(L) · LIR(L))
+ (Q3(L) · Q2(L) · Q1(H) · ALE(L) · 74ADDR(L)
· LIR(L))
+ (Q3(L) · Q2(L) · Q1(L) · Q0(H) · ALE(L)
· 74ADDR(L) · LIR(L))
+ (Q3(L) · Q2(H) · Q0(H)) + (RESET(H))

2. Q2(L) = (Q3(H) · Q2(H) · Q1(L) · Q0(H) · ALE(L)
· 74ADDR(L) · LIR(L) · RESET(L))
+ (Q3(H) · Q2(L) · Q1(L) · Q0(H) · ALE(L)
· 74ADDR(L) · LIR(L) · RESET(L))
+ (Q3(H) · Q2(L) · Q1(H) · Q0(H) · ALE(L)
· 74ADDR(L) · LIR(L) · RESET(L))

Table 4-21. Cascade Address PAL U30 Programming (Cont'd.)

2.	Q2(L) (Continued)	+ (Q3(H) · Q2(L) · Q1(H) · Q0(L) · ALE(L) · 74ADDR(L) · LIR(L) · RESET(L))
		+ (Q3(L) · Q2(L) · Q1(H) · Q0(L) · ALE(L) · 74ADDR(L) · LIR(L) · RESET(L))
		+ (Q3(L) · Q2(L) · Q1(H) · Q0(H) · ALE(L) · 74ADDR(L) · LIR(L) · RESET(L))
3.	Q1(L)	= (Q3(H) · Q2(H) · Q1(H) · Q0(L) · ALE(L) · RESET(L))
		+ (Q3(H) · Q2(H) · Q1(L) · Q0(L) · ALE(L) · 74ADDR(L) · LIR(L) · RESET(L))
		+ (Q3(H) · Q2(H) · Q1(L) · Q0(H) · ALE(L) · 74ADDR(L) · LIR(L) · RESET(L))
		+ (Q3(L) · Q2(L) · Q1(H) · Q0(H) · ALE(L) · 74ADDR(L) · LIR(L) · RESET(L))
		+ (Q3(L) · Q2(L) · Q1(L) · Q0(H) · ALE(L) · 74ADDR(L) · LIR(L) · RESET(L))
		+ (Q3(L) · Q2(H) · Q1(L) · Q0(H) · ALE(L) · RESET(L))
4.	Q0(L)	= (Q3(L) · Q2(H) · Q1(H) · Q0(H) · LIR(L) · RESET(L))
		+ (Q3(L) · Q2(H) · Q1(H) · Q0(L) · RESET(L))
		+ (Q3(H) · Q2(H) · Q1(H) · Q0(L) · ALE(L) · 74ADDR(L) · LIR(L) · RESET(L))

Table 4-21. Cascade Address PAL U30 Programming (Cont'd.)

4.	Q0(L) (Continued)	+ (Q3(H) · Q2(L) · Q1(H) · Q0(H) · ALE(L) · 74ADDR(L) · LIR(L) · RESET(L))
		+ (Q3(H) · Q2(L) · Q1(H) · Q0(L) · ALE(L) · 74ADDR(L) · LIR(L) · RESET(L))
5.	74INTA(L)	= (Q3(H) · Q2(H) · Q1(L))
		+ (Q3(L) · Q2(L))
		+ (Q3(H) · Q1(L) · Q0(H))
6.	LOCAL DEN(L)	= (Q3(H) · Q2(H) · Q1(L))
		+ (Q2(L))
		+ (PCS1(L) · 80130 I/O CS(H))
7.	INT1 S(L)	= AA(H) · A9(L) · A8(L) · LIR(L)
8.	74ADDR	= AA(L) · A9(H) · A8(H) · ALE(L)

Table 4-22. Cascade Address State Machine

STATES	OUTPUTS			CURRENT STATE	INPUT(1) 000	INPUT(1) 001	INPUT(1) 010	INPUT(1) 011
	8274 INTA/	LOCAL DEN/	U30-14 Interrupt Wait	Q3 Q2 Q1 Q0	Q3 Q2 Q1 Q0	Q3 Q2 Q1 Q0	Q3 Q2 Q1 Q0	Q3 Q2 Q1 Q0
Wait For LIR/	OFF	OFF	OFF	1 0 0 0	1 0 0 0	1 0 0 1	1 0 0 0	1 0 0 1
Wait For ALE	OFF	OFF	OFF	1 0 0 1	1 0 0 1	1 0 0 1	1 0 0 1	1 0 0 1
Delay 1 Clock	ON	OFF	ON	0 0 0 1	1 0 1 0	1 0 1 0	1 0 1 0	0 0 1 1
First 8274 INTA	ON	ON	ON	0 0 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 0
First 8274 INTA	ON	ON	ON	0 0 1 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 1 0
INTA OFF	OFF	ON	ON	0 1 1 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 0
INTA Off	OFF	ON	ON	0 1 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 1 0 1
INTA Off	OFF	ON	ON	0 1 0 1	0 0 0 0	0 0 0 0	0 0 0 0	1 1 0 1
Second 8274 INTA	ON	ON	OFF	1 1 0 1	0 0 0 0	0 0 0 0	0 0 0 0	1 1 0 0
Second 8274 INTA	ON	ON	OFF	1 1 0 0	0 0 0 0	0 0 0 0	0 0 0 0	1 1 1 0
Second 8274 INTA	ON	ON	OFF	1 1 1 0	0 0 0 0	0 0 0 0	0 0 0 0	1 0 1 0
Cycle Complete	OFF	OFF	OFF	1 0 1 0	1 0 1 0	1 0 1 0	1 0 1 0	1 0 1 0
Error State	OFF	OFF	ON	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Invalid States	X	X	X	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Invalid States	X	X	X	0 1 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Invalid States	X	X	X	1 1 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

NOTES: 1. INPUTS X X X
= LIR
= ADDR = (AA · A9 · A8 · LIR)
= ALE

2. Table assumes positive logic
3. Reset will return to 1000 states

Table 4-22. Cascade Address State Machine (Cont'd.)

STATES	OUTPUTS			CURRENT STATE	INPUT(1) 100	INPUT(1) 101	INPUT(1) 110	INPUT(1) 111
	8274 INTA/	LOCAL DEN/	U30-15 Interrupt Wait	Q3 Q2 Q1 Q0	Q3 Q2 Q1 Q0	Q3 Q2 Q1 Q0	Q3 Q2 Q1 Q0	Q3 Q2 Q1 Q0
Wait For LIR/	OFF	OFF	OFF	1 0 0 0	1 0 0 0	1 0 0 1	1 0 0 0	1 0 0 1
Wait For ALE	OFF	OFF	OFF	1 0 0 1	1 0 1 1	1 0 1 1	1 0 1 1	1 0 1 1
Delay 1 Clock	OFF	OFF	ON	1 0 1 1	1 0 1 0	0 0 0 0	0 0 0 0	0 0 0 0
First 8274 INTA	ON	ON	ON	0 0 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
First 8274 INTA	ON	ON	ON	0 0 1 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
INTA OFF	OFF	ON	ON	0 1 1 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
INTA Off	OFF	ON	ON	0 1 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
INTA Off	OFF	ON	ON	0 1 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Second 8274 INTA	ON	ON	OFF	1 1 0 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Second 8274 INTA	ON	ON	OFF	1 1 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Second 8274 INTA	ON	ON	OFF	1 1 1 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Cycle Complete	OFF	OFF	OFF	1 0 1 0	1 0 0 0	1 0 0 0	1 0 0 0	1 0 0 0
Error State	OFF	OFF	ON	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Invalid States	X	X	X	1 0 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Invalid States	X	X	X	0 1 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
Invalid States	X	X	X	1 1 1 1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

NOTES: 1. INPUTS X X X
= LIR
= ADDR = (AA · A9 · A8 · LIR)
= ALE

2. Table assumes positive logic
3. Reset will return to 1000 states

4.4.5 80186 VECTORED INTERRUPT CYCLE

When the 80186 is to generate the interrupt vector, it asserts SLAVINT (INTA1/) to the 80130A device as IR4 (Interrupt Request 4). In response to SLAVE INT the 80130A device asserts INT0 back to the 80186. At this point the 80186 asserts ~~ interrupt acknowledge status (S0/, S1/ and S2/).

The status bits are monitored by both the 80130A and the 8288. The 8288 asserts ALE which latches address bits AA, A8 and A9 driven by the 80130A. PAL U30 decodes the bits and generates INT1 SLV SEL/ to the 80186 which puts the vector on the data bus at the next clock.

4.4.6 DMA OPERATION

DMA transfers on the iSBC 186/51S can occur memory to memory, I/O to I/O or memory to I/O. The memory and/or the I/O can be on-board or on the MULTIBUS Interface.

The 80186 processor has two DMA request lines DRQ0 and DRQ1. The DMA requests that can be connected to these inputs are determined by a set of stake pins as shown below:

80186 DMA Request Input	Stake Pins	Signal and Source
DRQ0	E67 to E70	RXDRQA, Serial Controller U2
DRQ0	E71 to E70	RXDRQB, Serial Controller U2
DRQ0	E72 to E70	MDRQT2, iSBX Connector J4
DRQ1	E27 to E24	TXDRQA, Serial Controller U2
DRQ1	E25 to E24	TXDRQB, Serial Controller U2
DRQ1	E21 to E24	MDRQT1, iSBX Connector J5

The 80186 processor does not have DMA acknowledge outputs. In place of these outputs a DMA cycle is always directed toward an I/O chip select or memory.

A DMA cycle consumes two to four bus cycles, a minimum of eight clocks. Data is read into the 80186 processor from the source and sent back out to the destination. Normal memory and/or I/O transfers are performed.

Two DMA acknowledge signals, MDACK1/ and MDACK2/ are generated, by a 74S138 decoder located at U27, for the two iSBX interfaces. The signals will be active under the conditions shown below:

U49-18	EARLY CMD	A3	A2	A1	
L	H	L	H	L	MDACK1/ low
L	H	L	H	H	MDACK2/ low

CHAPTER 5. SERVICE INFORMATION

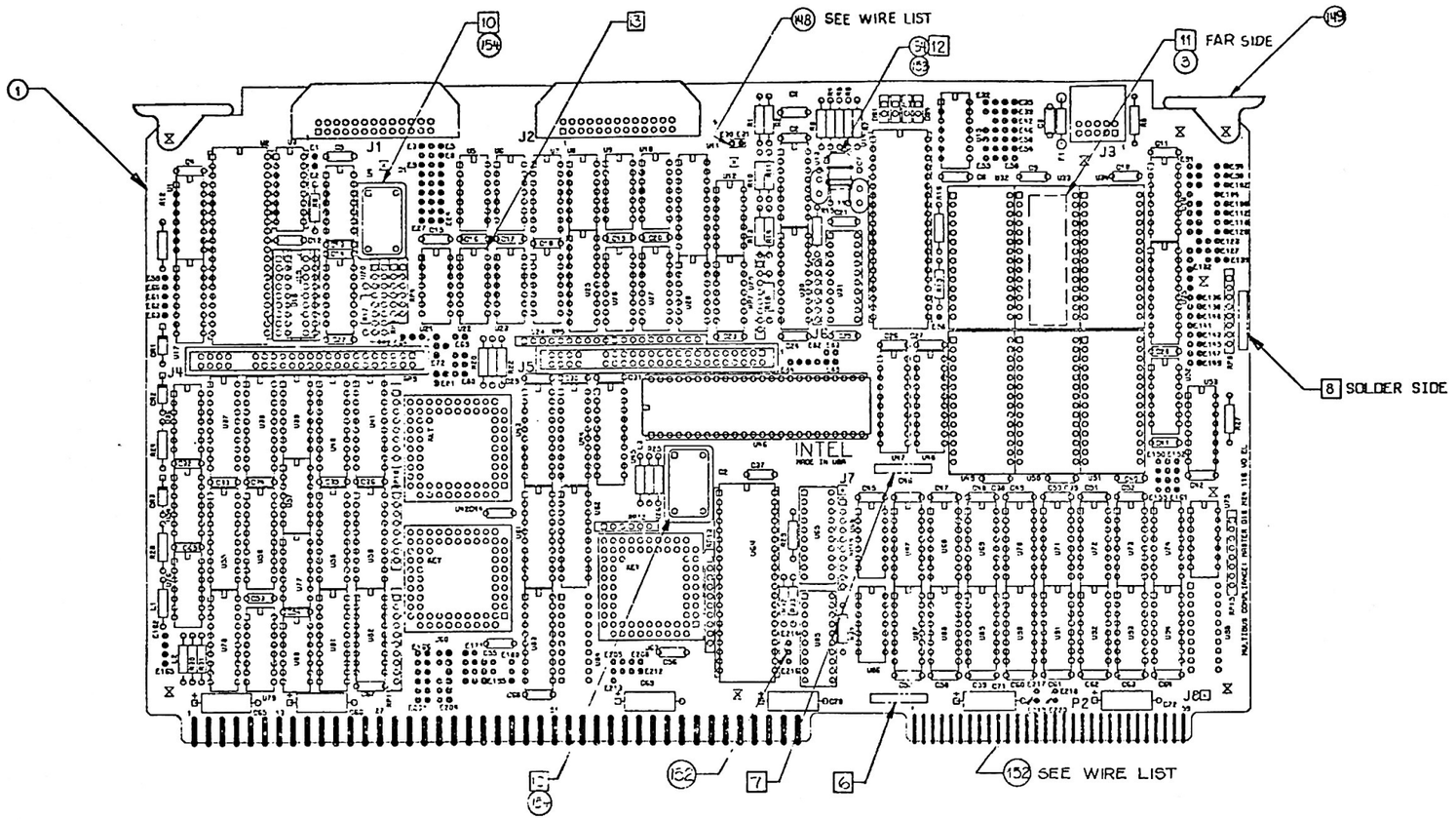
5.1 Introduction

This chapter provides a parts location diagram, service diagram, and service and repair assistance instructions for the iSBC 186/51S board and the MB502A Adaptor Board.

5.2 Service Diagrams

The iSBC 186/51S board parts location drawing and schematic diagram are provided in Figures 5-1 and 5-3. Table 5-1 locates, by sheet numbers, the reference designators on Figure 5-3. The MB502A board parts location drawing and schematic diagram are provided in Figures 5-2 and 5-4. Signal mnemonics ending with slashes (e.g., PROC LOCK/) indicate active low operation. Conversely, mnemonics without slashes (e.g., 16M CLK) indicate active high operation.

The schematic diagrams are current when the manual is printed. However, minor revisions to the diagrams may occur between manual printings. Therefore, Intel provides copies of the current schematic diagrams with the board when it is shipped from the factory. These diagrams should be inserted into this manual for future reference.



NOTES: UNLESS OTHERWISE SPECIFIED

1. ASSEMBLY PART NUMBER IS 146974-001
2. THIS DOCUMENT, PARTS LIST AND WIRE LIST ARE TRACKING DOCUMENTS.
3. WORKMANSHIP PER INTEL 99-0007-001.
4. MAXIMUM HEIGHT OF COMPONENTS SHALL BE .40 INCH FROM BOARD SURFACE.
5. MAXIMUM HEIGHT OF LEADS ON SOLDER SIDE SHALL BE .09 INCH FROM BOARD SURFACE.

[6] MARK 'PBA' AND PART NUMBER IN CONTRASTING PERMANENT COLOR NON-CONDUCTIVE, .06 INCH HIGH MINIMUM CHARACTERS APPROXIMATELY WHERE SHOWN.

[7] MARK PRODUCT CODE AND SERIAL NUMBER IN CONTRASTING PERMANENT COLOR NON-CONDUCTIVE, .06 INCH HIGH MINIMUM CHARACTERS APPROXIMATELY WHERE SHOWN.

[8] MARK ASSEMBLY VENDOR ID IN CONTRASTING PERMANENT COLOR, NON-CONDUCTIVE, .08 INCH HIGH MINIMUM CHARACTERS APPROXIMATELY WHERE SHOWN.

9. SOCKET REFERENCE DESIGNATIONS ARE COMPONENT REFERENCE DESIGNATIONS PREFIXED WITH X .

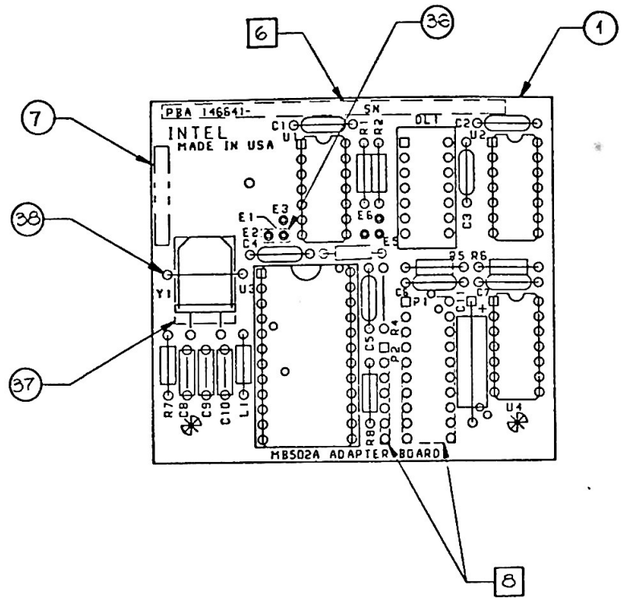
[10] INSTALL FOAM TAPE UNDER OSCILLATOR.

[11] INSTALL ITEM 3 ON SOLDER SIDE AT XU33 SO THAT IC PADS ARE FREE OF LABEL AND ADHESIVE.

[12] INSTALL FOAM TAPE UNDER CRYSTAL, AND STRAP AS SHOWN.

[13] CUT U22 PINS 11 AND 13 FLUSH WITH BODY.

Figure 5-1. iSBC® 186/51S Board Component Location Diagram



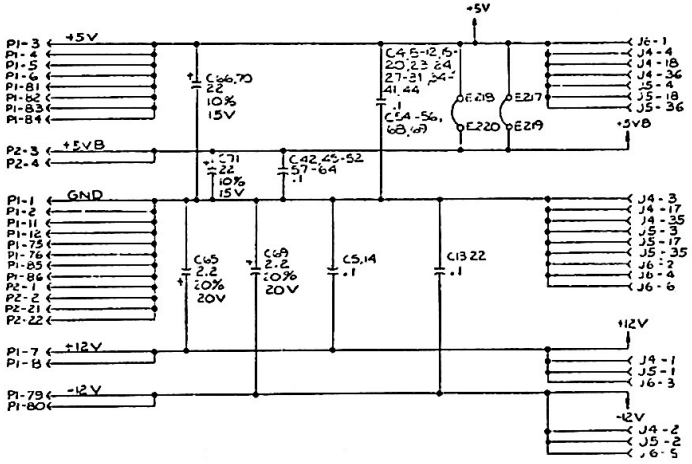
NOTES; UNLESS OTHERWISE SPECIFIED:

1. ASSEMBLY PART NUMBER IS 146641-001.
2. THIS DOCUMENT AND PARTS LIST ARE TRACKING DOCUMENTS.
3. WORKMANSHIP PER INTEL 99-0007-001.
4. MAXIMUM HEIGHT OF COMPONENTS SHALL BE .40 INCH FROM BOARD SURFACE.
5. MAXIMUM HEIGHT OF LEADS ON SOLDER SIDE SHALL BE .09 INCH FROM BOARD SURFACE.
6. MARK "PBA", PART NUMBER AND SERIAL NUMBER IN CONTRASTING PERMANENT COLOR, NON-CONDUCTIVE, .08 INCH MINIMUM HIGH CHARACTERS APPROXIMATELY WHERE SHOWN.
7. MARK ASSEMBLY VENDOR IDENTIFICATION IN CONTRASTING PERMANENT COLOR, NON-CONDUCTIVE, .08 INCH MINIMUM HIGH CHARACTERS APPROXIMATELY WHERE SHOWN.
8. INSTALL SOCKET ADAPTERS, ITEMS 29 AND 31, FROM SOLDER SIDE INSERTING THE LARGER DIAMETER PINS INTO P2 AND P1 HOLE PATTERNS RESPECTIVELY; THEN INSERT ITEMS 29 AND 31 INTO SOCKETS, ITEMS 28 AND 30.

Figure 5-2. MB502A Adapter Board Component Location Diagram

Table 5-1. Reference Designator Locator Table

Designator	Schematic Sheet	Designator	Schematic Sheet	Designator	Schematic Sheet	Designator	Schematic Sheet
U 1	11	U29	2	U57	8	U85	7
U 2	8	U30	3	U58	4	U86	4,5,6,8
U 3	11	U31	2	U59	8	U87	7
U 4	8	U32	9	U60	4,6	U88	7
U 5	3	U33	9	U61	4	U89	7
U 6	4,8	U34	9	U62	5	U90	7
U 7	10	U35	7,10	U63	7	U91	7
U 8	6,9,10	U36	3,6	U64	7	U92	7
U 9	3,5,7	U37	6	U65	7	U93	7
U10	2,4,10	U38	3	U66	6,7	U94	7
U11	10	U39	6	U67	7		
U12	4,6	U40	3	U68	7		
U13	3,10	U41	8	U69	7		
U14	3	U42	2	U70	7		
U15	2,3,10	U43	7	U71	7		
U16	6	U44	7	U72	7		
U17	10	U45	4	U73	7		
U18	11	U46	2	U74	7		
U19	11	U47	3,10	U75	5		
U20	11	U48	4	U76	2,4		
U21	2,3,4	U49	9	U77	8		
U22	2,7	U50	9	U78	3,6,10		
U23	4,7,8	U51	9	U79	3,5		
U24	2,4	U52	7	U80	5		
U25	4	U53	8	U81	4		
U26	10	U54	2,5,6	U82	5		
U27	8	U55	3,4,5	U83	10		
U28	2,3,5,7,10	U56	6,7	U84	-		



DEVICE TABLE							
REFERENCE DESIGNATIONS	DEVICE TYPE	POWER PINS GND	+5V	+5VB	+12V	-12V	UNUSED LOGIC ELEMENT OUTPUT PINS
U1,7-74,77-79	2164	16		8			
U62	[illegible]	9	18				
U64	8203	20		[illegible]			
U2	8274	20	40				
U47	8283	10	20				
U43,44	8284	10	20				
U25,81	8283	10	20				
U65	8289	10	20				
U14	80130	20	40				
U22	80186	26,60	9,43				
U30	82284	26,60	9,43				
U60	PLT5322A	26,60	9,43				
U3	PSI 2431	10	20				
U20	PAL 14H4	10	20				
U13,36,38	PAL 16R4	10	20				
U63	PAL 16L8	10	20				
U37,41,56	PAL 16L8	10	20				
U9	[illegible]	[illegible]	16				
U4,20	488	7			14	1	
U6	1488	7	14				
U1	3486	8	16				
U3	1487	8	16				
U58	74S00	7		14			
U77	74S00	7	14				
U9	74S02	7	14				
U21,28	74S04	7	14				
U23	74LS04	7	14				
U5	7406	7	14				
U22	74S08	7	14				
U26	74F10	7	14				
U24	74LS20	7	14				
U9	74S32	7	14				
U16	74LS32	7		14			
U57	74S74	7	14				
U79	74S112	8	16				
U 3	74LS123	8	16				
U52	74LS125	7	14				
U76	74125	7	14				
U54	74LS132	7	14				
U27	74S138	8	16				
U53	74S139	8	16				
U29	74LS[illegible]	7	14				U27-8
U59	74S175	8	16				U29-14,15
U78	74LS240	10	20				U75-10,15
U55	74LS241	10	20				U55-7
U33	74LS244	10	20				U55-3
U46	74LS[illegible]59	8	16				
U75,80	74LS266	7	14				U80-10,11
U7	74LS279	8	16				
U17	74S288	8	16				
U16	74367	8	16				U16-5,7,9
U48	74S373	10	20				
U45,61	74S374	10	20				
U74	74LS30	7	14				
U66,69	PAL 20A	10	20				
U8	8284A	18	[illegible]				
U5	74LS14	7	14				U5-10
U34	SPARE	5	20				
U35	SPARE	10		20			

NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITANCE VALUES ARE IN MICROFARADS, +80%,-20%,-50V.
2. RESISTANCE VALUES ARE IN OHMS, 1/4 W, 5%.

3 CUSTOMER SUPPLIED AND INSTALLED.

4 COMPONENT VALUE TO BE DETERMINED BY THE CUSTOMER.

5 THIS FUNCTION PROVIDED BY EMULATOR BOARD SEE SCHEMATIC 1-C243.

Figure 5-3. iSBC® 186/51S Board Schematic Diagram (Sheet 1 of 12)

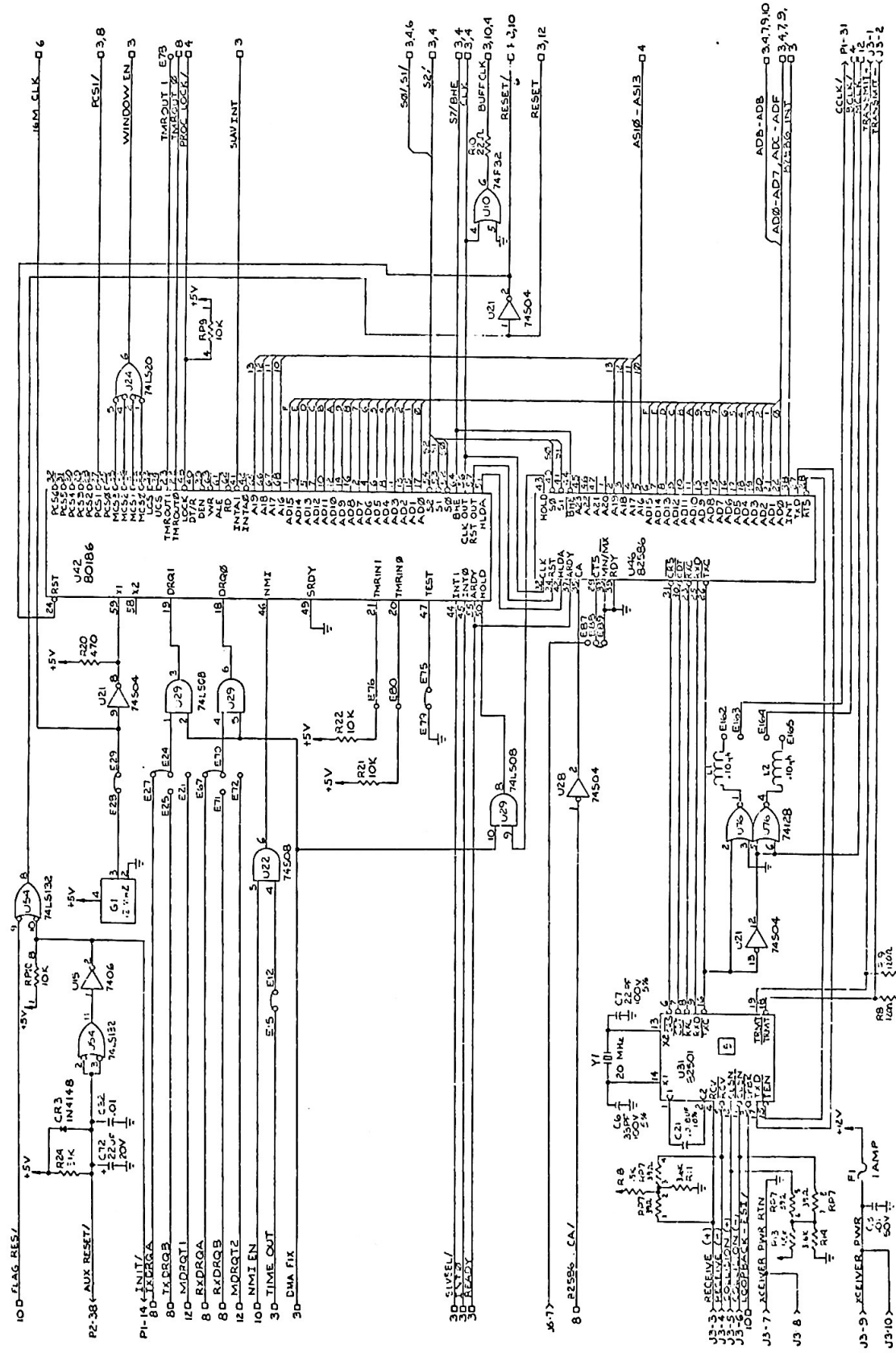


Figure 5-3. iSBC® 186/51S Board Schematic Diagram (Sheet 2 of 12)

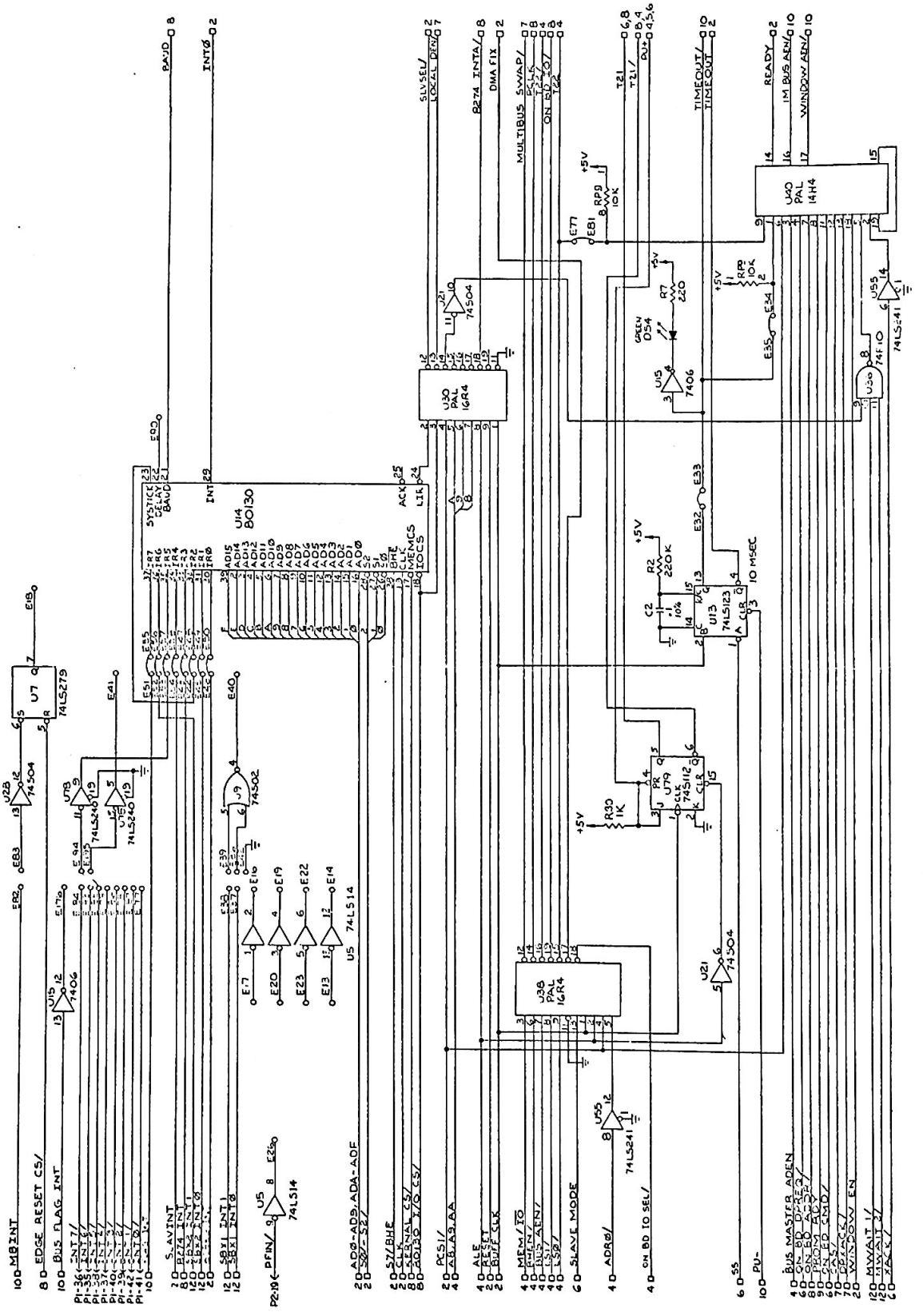


Figure 5-3. iSBC® 186/51S Board Schematic Diagram (Sheet 3 of 12)

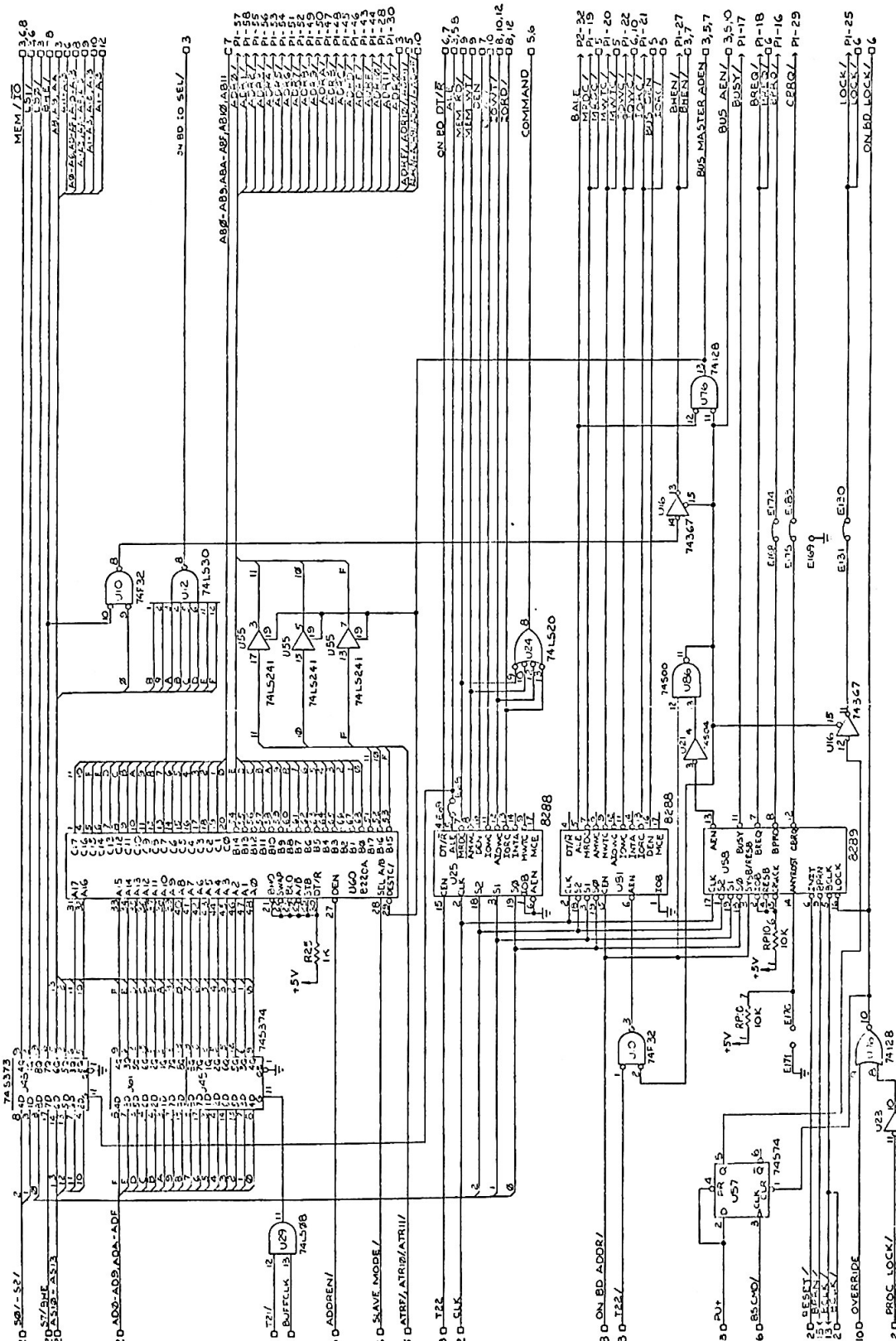


Figure 5-3. iSBC® 186/51S Board Schematic Diagram (Sheet 4 of 12)

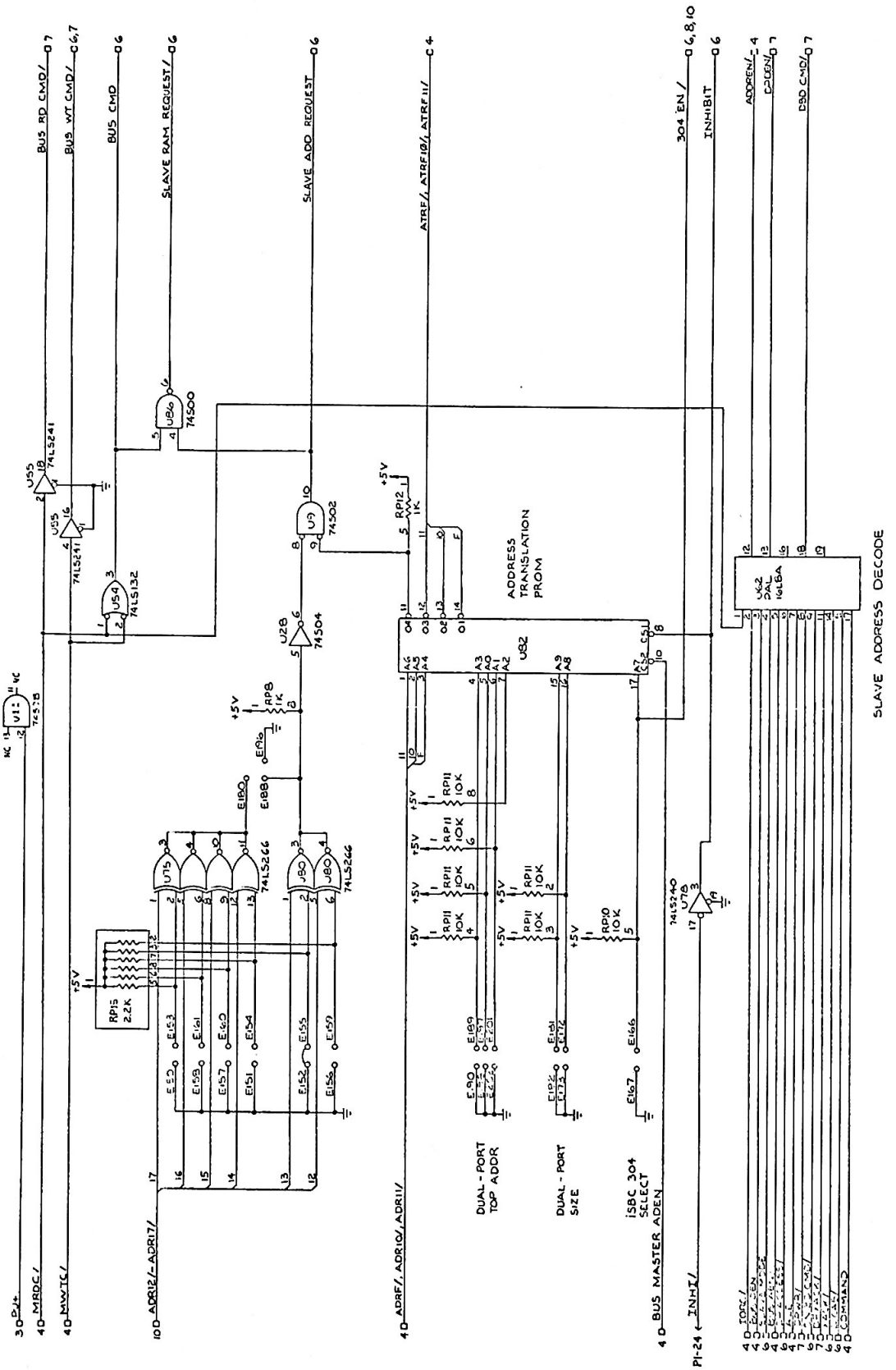


Figure 5-3. iSBC® 186/51S Board Schematic Diagram (Sheet 5 of 12)

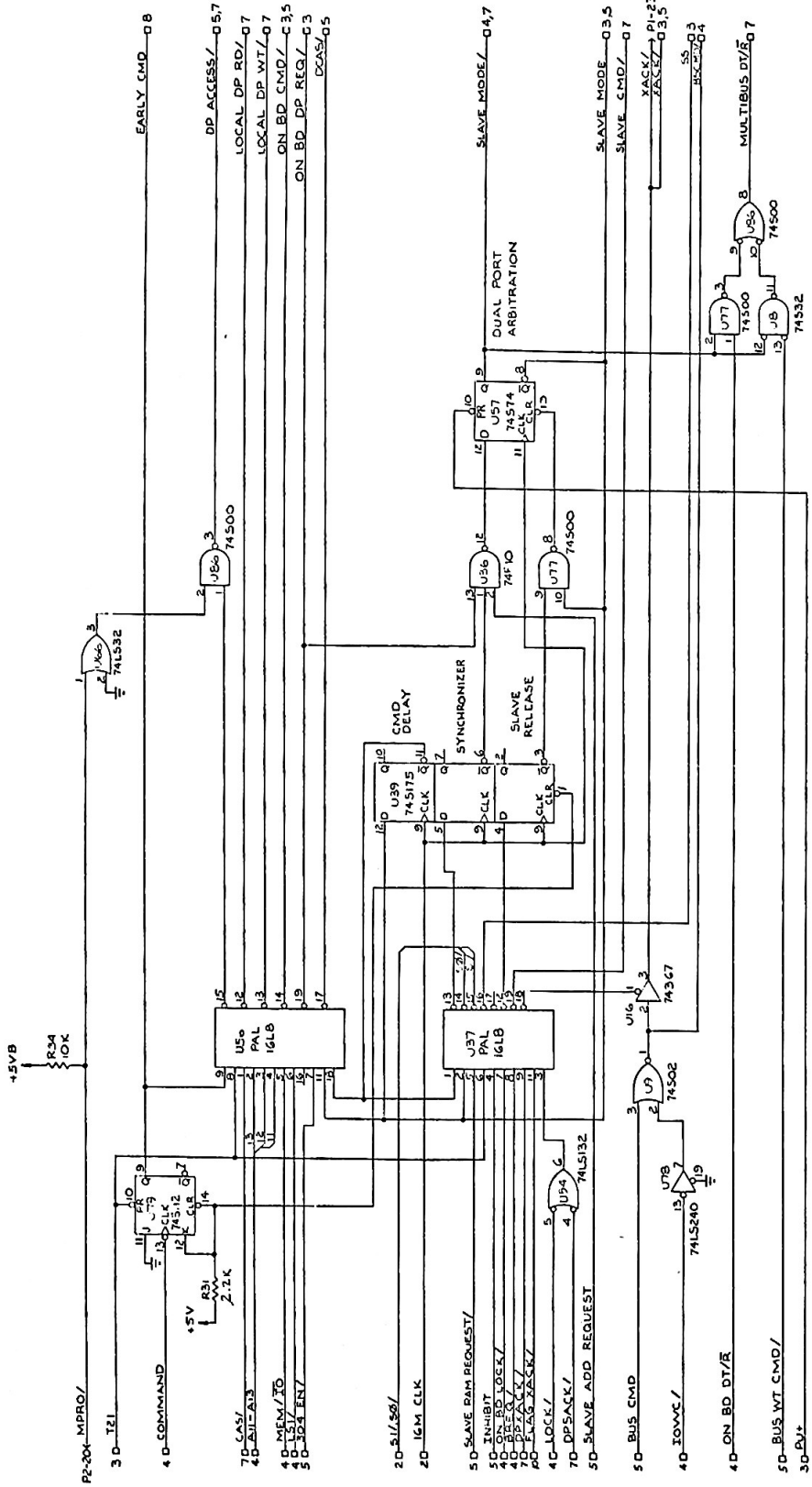


Figure 5-3. iSBC® 186/51S Board Schematic Diagram (Sheet 6 of 12)

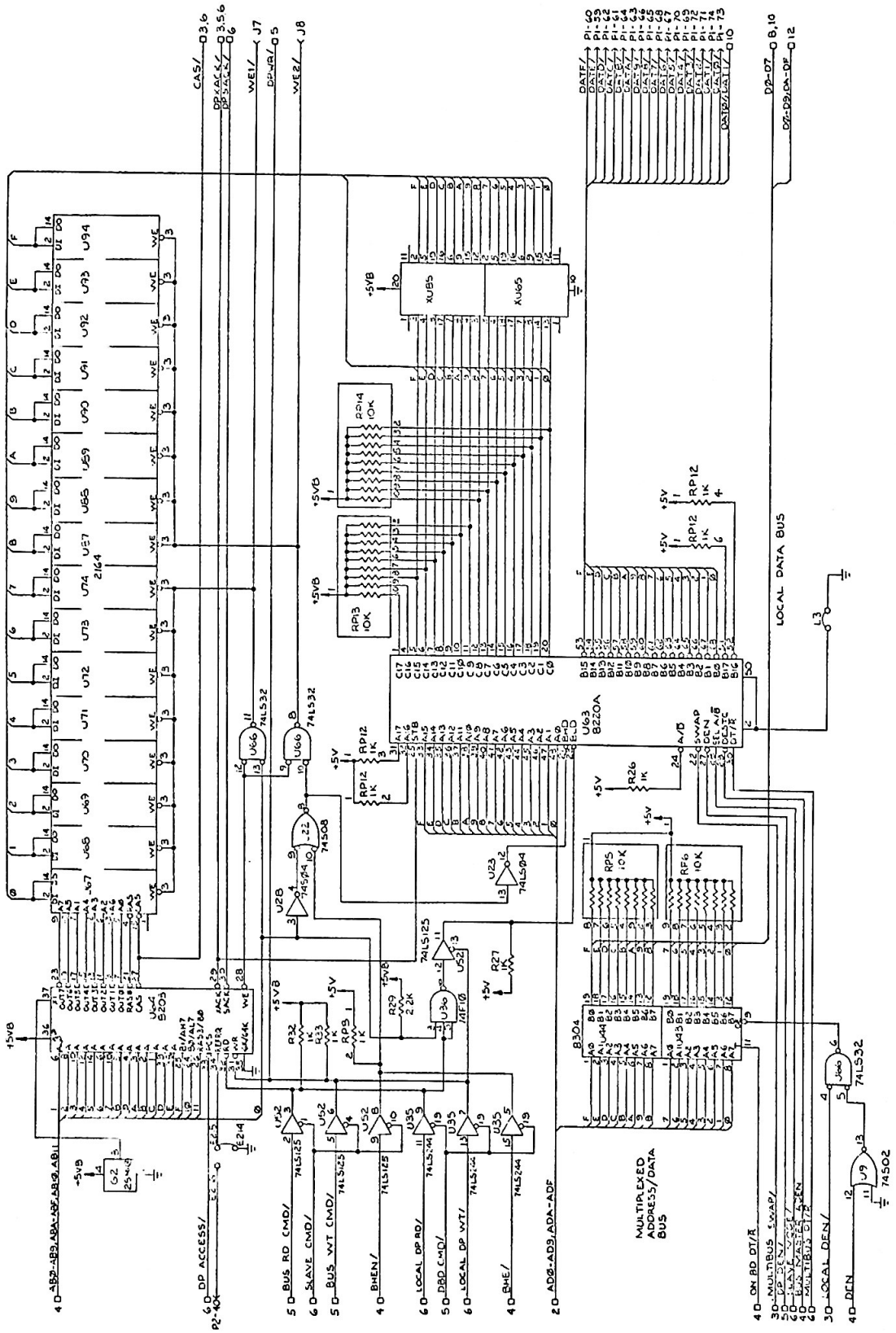


Figure 5-3. iSBC® 186/51S Board Schematic Diagram (Sheet 7 of 12)

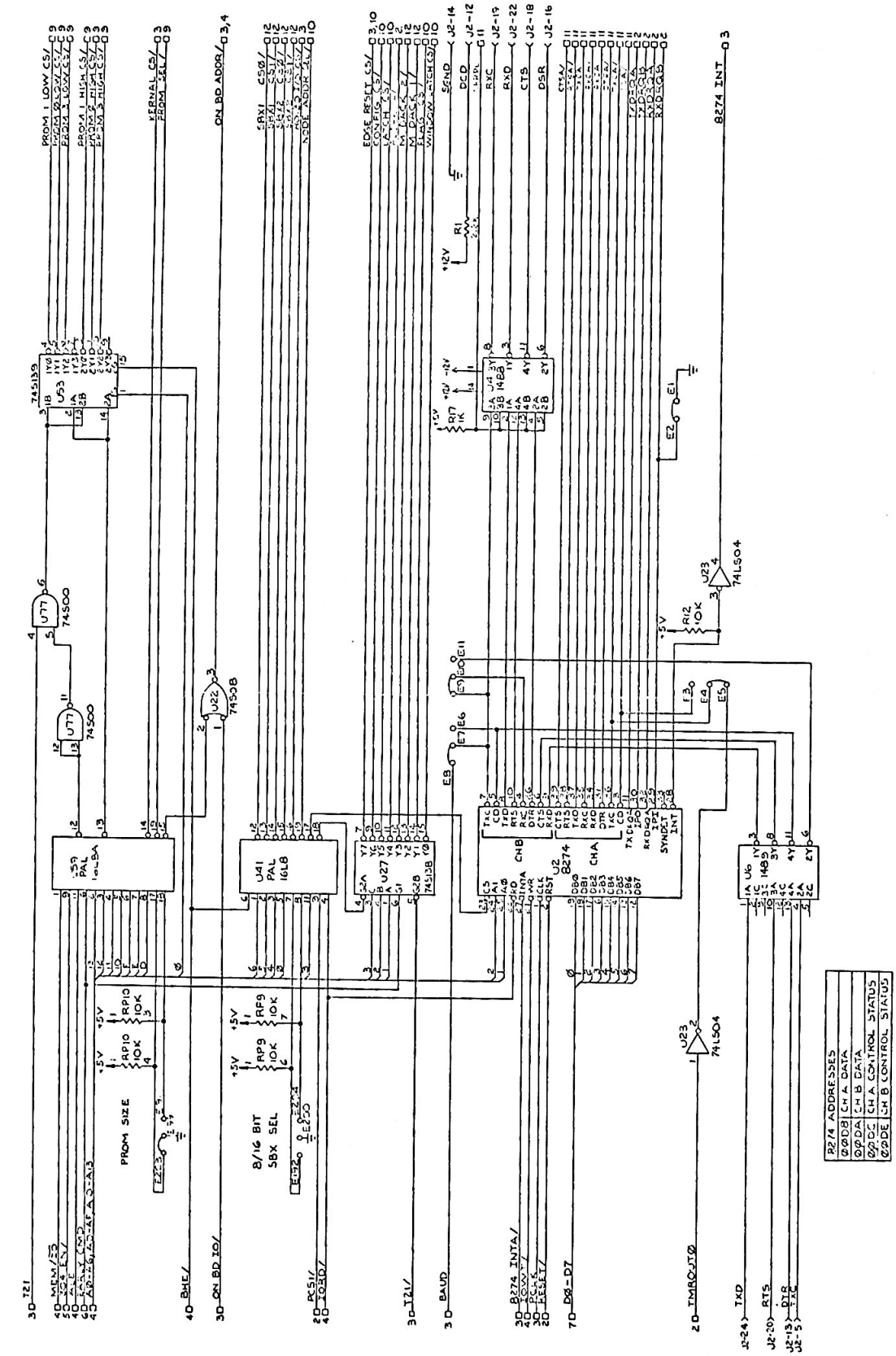


Figure 5-3. iSBC® 186/51S Board Schematic Diagram (Sheet 8 of 12)

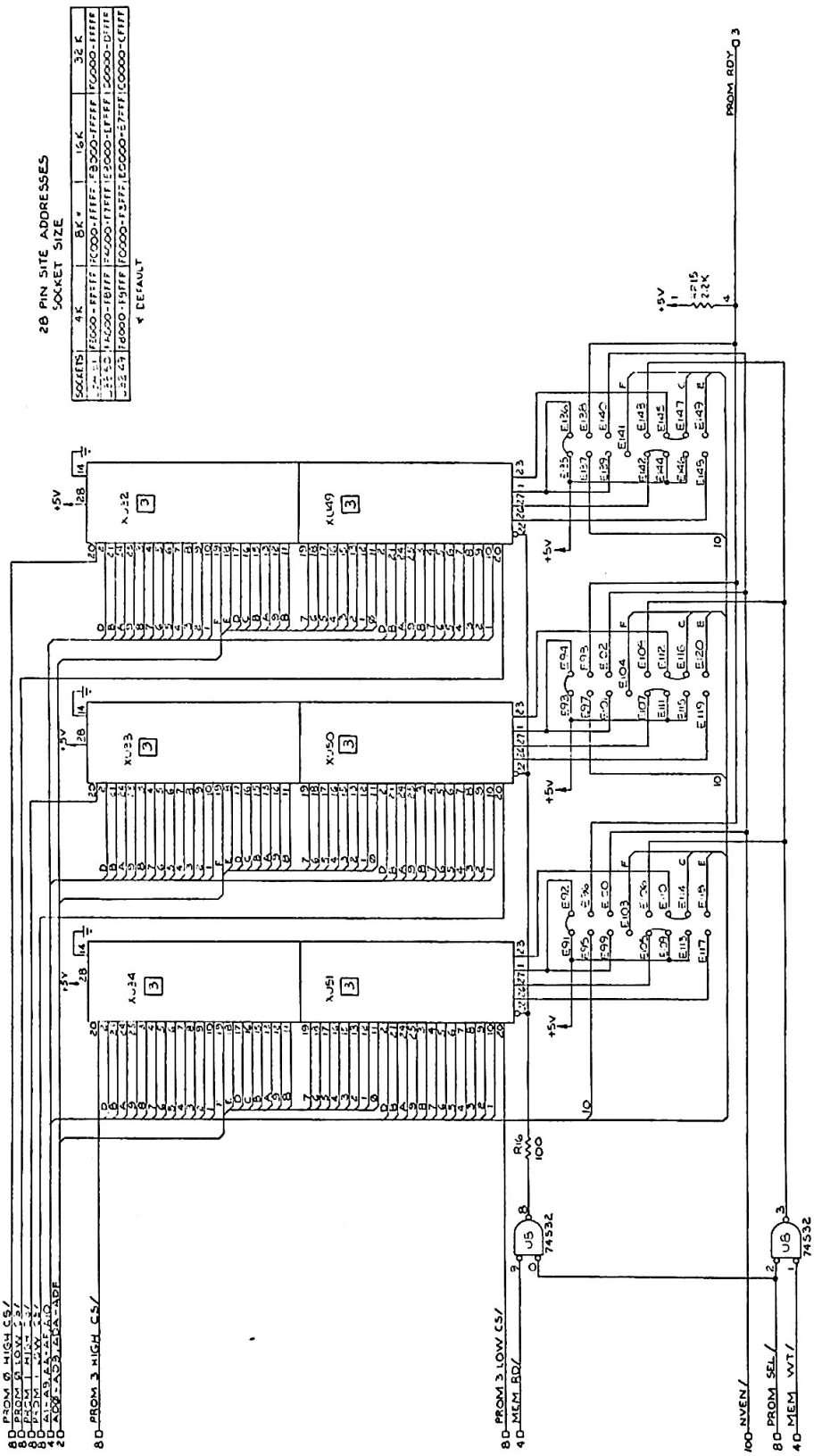


Figure 5-3. iSBC® 186/51S Board Schematic Diagram (Sheet 9 of 12)

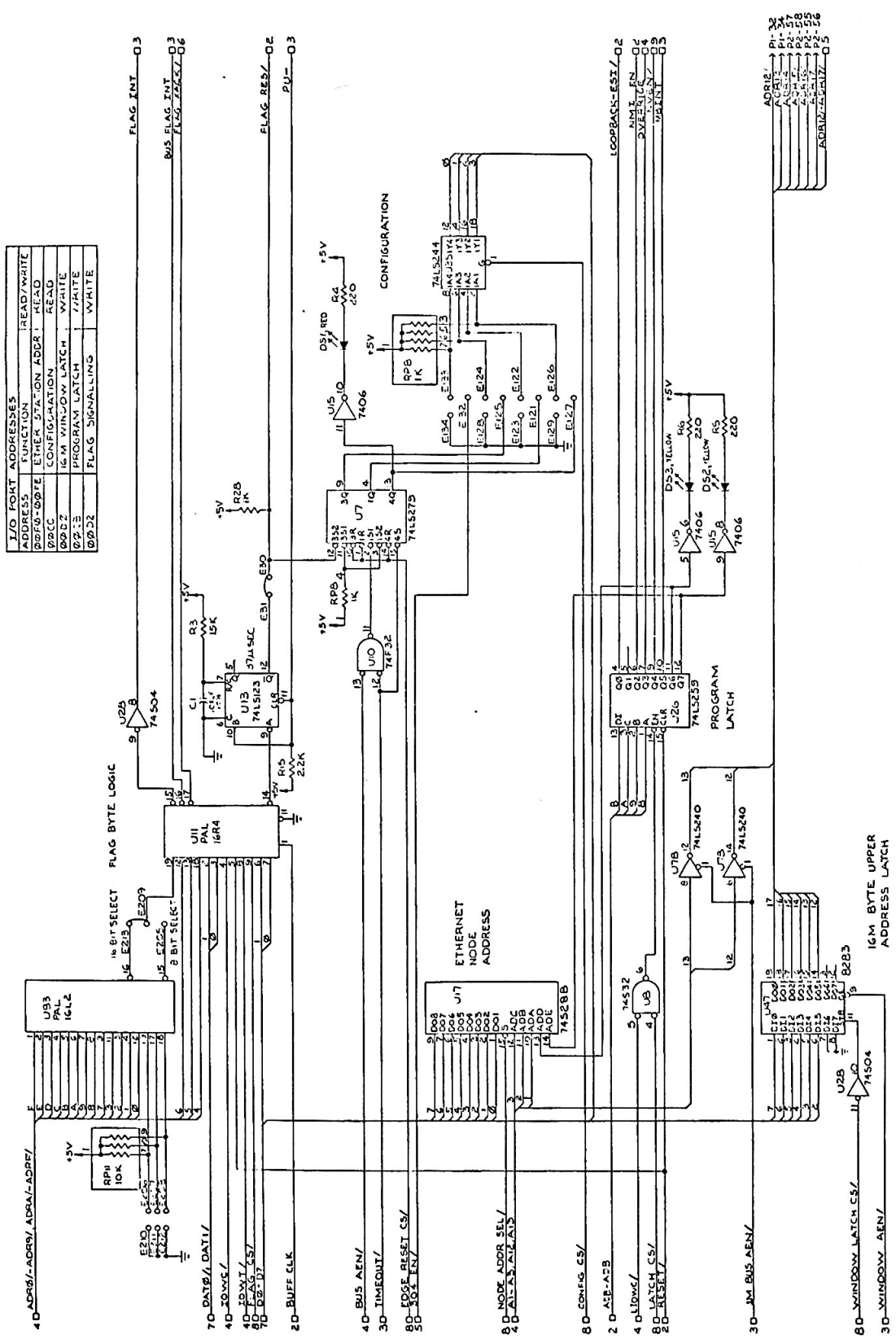


Figure 5-3. iSBC® 186/51S Board Schematic Diagram (Sheet 10 of 12)

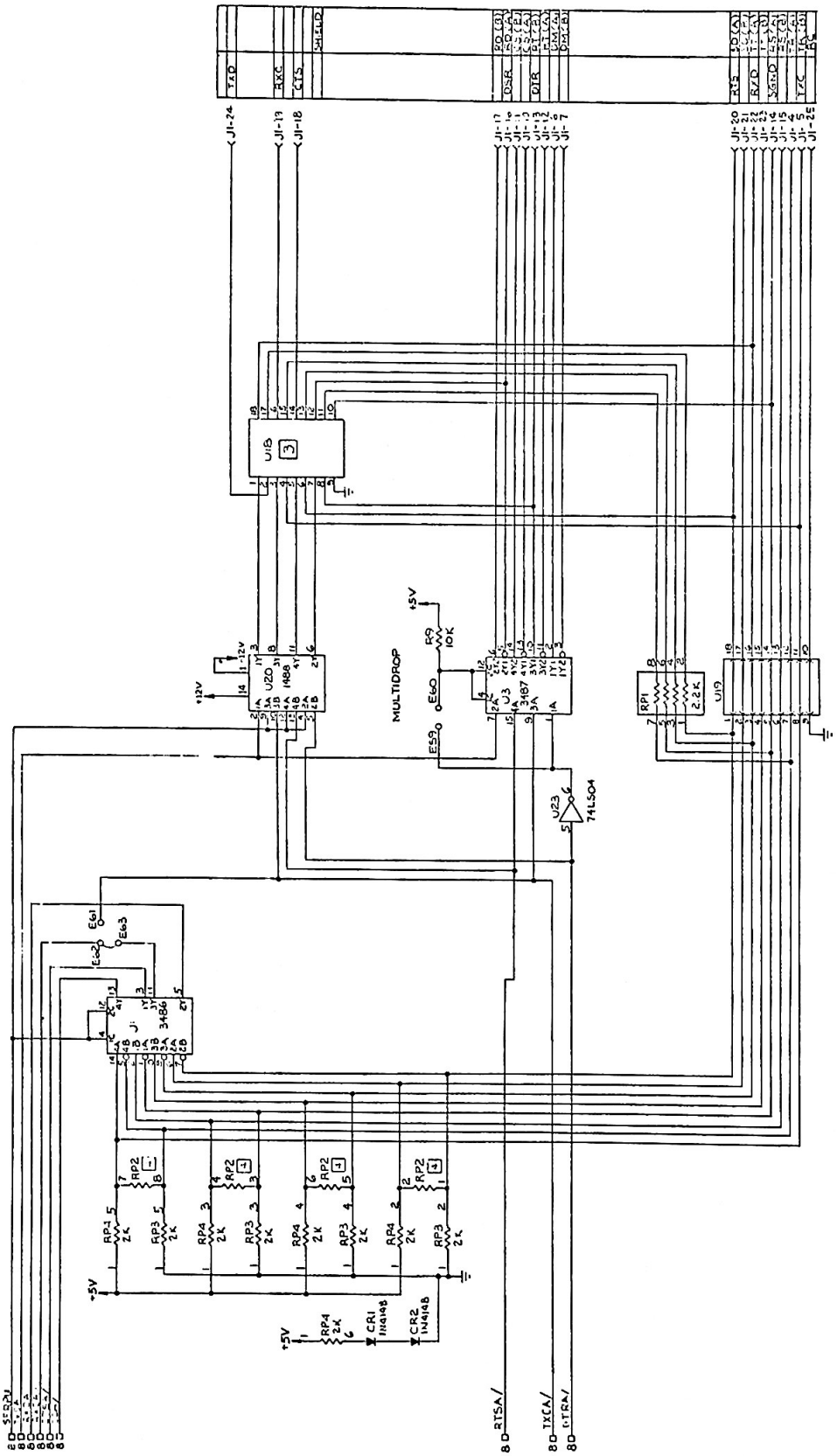


Figure 5-3. iSBC® 186/51S Board Schematic Diagram (Sheet 11 of 12)

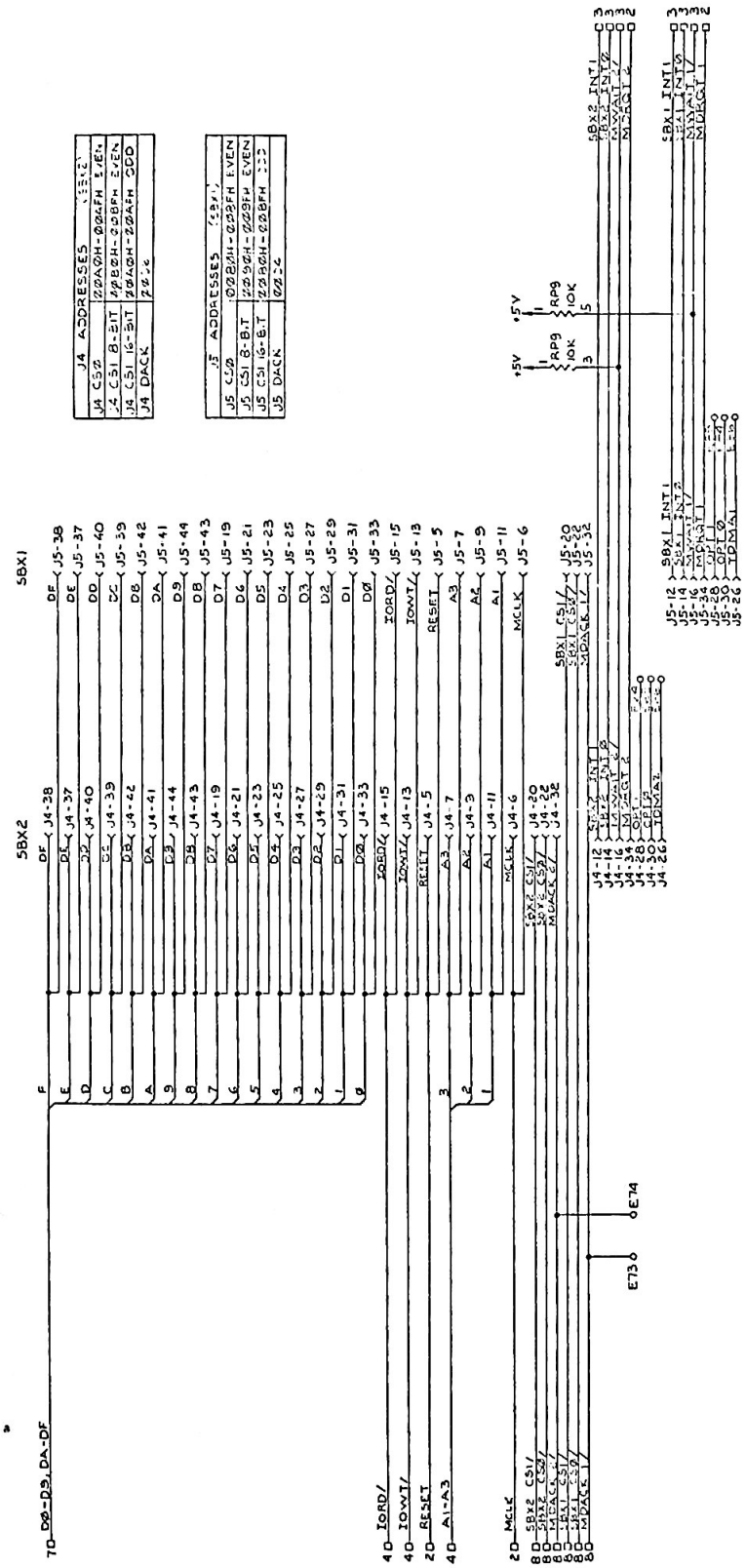
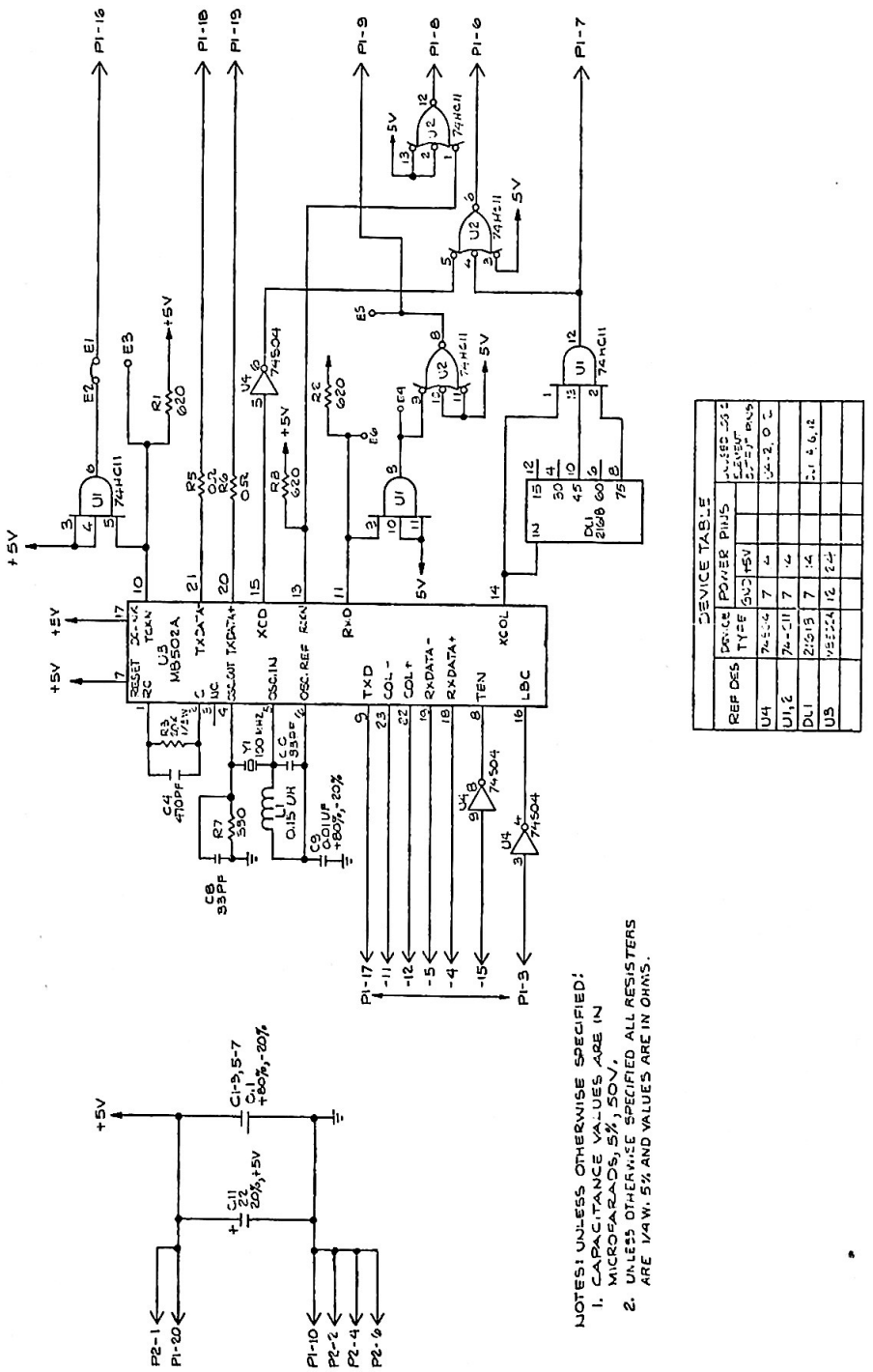


Figure 5-3. iSBC® 186/51S Board Schematic Diagram (Sheet 12 of 12)



NOTES: UNLESS OTHERWISE SPECIFIED:
1. CAPACITANCE VALUES ARE IN MICROFARADS, 5%, 50V.
2. UNLESS OTHERWISE SPECIFIED ALL RESISTERS ARE 1/4 W. 5% AND VALUES ARE IN OHMS.

Figure 5-4. MB502A Adapter Board Schematic Diagram

5.3 Service and Repair Assistance

United States customers can obtain service and repair assistance by contacting the Intel Product Service Hotline in Phoenix, Arizona. Customers outside the United States should contact their sales source (Intel Sales Office or authorized distributor) for service information and repair assistance.

Before calling the Product Service Hotline, you should have the following information available.

1. Date you received the product.

2. Complete part number of the product (including the dash number). This number is usually silk-screened on the board.

3. Serial number of the product. This number is stamped on the board.

4. Shipping and billing addresses.

5. If your Intel product warranty has expired, you must provide a purchase order number for billing purposes.

6. If you have an extended warranty agreement, be sure to advise the Hotline personnel of this agreement.

Use the following numbers for contacting the Intel Product Service Hotline.

Regional Telephone Numbers:

Western Region	602-869-4862
Midwestern Region	602-869-4392
Eastern Region	602-869-4045
International	602-869-4391
TWX Numbers	910-951-1330
	910-951-0687

Always contact the Product Service Marketing Administration Group before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions and other important information that will help Intel to provide you with fast efficient service. If you are returning the product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to Intel, use the original factory packing material, if possible. If this material is not available, wrap the product in a cushioning material such as Air Cap TH-240 manufactured by the Sealed Air Corporation, Hawthorne, New Jersey. Then, pack it in a heavy corrugated paper shipping carton and label it "FRAGILE" to ensure careful handling. Ship it only to the address specified by Product Service Marketing Administration personnel.

APPENDIX A. iSBC® 304 RAM EXPANSION MULTIMODULE™ BOARD INSTALLATION

A.1 Introduction

This appendix provides information for installing the iSBC 304 RAM Expansion MULTIMODULE Board (see Figures A-2 and A-3) that may be installed on the iSBC 186/51S Board.

A.2 iSBC® 304 Board Installation

The following steps explain how to unpack and install the iSBC 304 board.

1. Unpack the board.
2. Inspect the board for damage. If any damage exists follow the instructions for repair as described in Chapter 5 of this manual.
3. Remove the iSBC 186/51S board from the backplane and place it (component side up) on a soft surface (preferably a piece of foam).
4. Remove the 8203 Dynamic RAM Controller IC located at U64 on the iSBC 186/51S board.

NOTE

Save the IC removed in Step 4. It will be re-installed later.

5. Insert the iSBC 304 board mating pins into the sockets at U64, U65 and U85, orienting the board as shown in Figure A-1.
6. Ensure that the mating pins are properly aligned and carefully press the iSBC 304 board into place by applying pressure at U1 of the iSBC 304 board.
7. Place the nylon spacer between the iSBC 186/51S board and the iSBC 304 board at one of the holes shown in Figure A-1.
8. Insert the screw from solder side through the iSBC 186/51S board, through the nylon spacer and the iSBC 304 board.
9. Attach the nut and tighten finger tight.

10. Repeat steps 7, 8, and 9 for the other two mounting holes.
11. When all spacers are in place tighten all three screws.

CAUTION

Do not overtighten the screws. Damage to the board could result.

12. Insert the 8203 IC, removed in Step 4, into location U1 on the iSBC 304 board. Location U1 is directly above U64 on the iSBC 186/51S board.

CAUTION

Ensure that the IC is properly oriented in its sockets or it could be damaged when power is applied.

13. Install jumper E176 to E202 on the iSBC 186/51S board. Refer to Tables 2-29 and 2-30 in this manual to configure the dual port RAM MULTIBUS address.

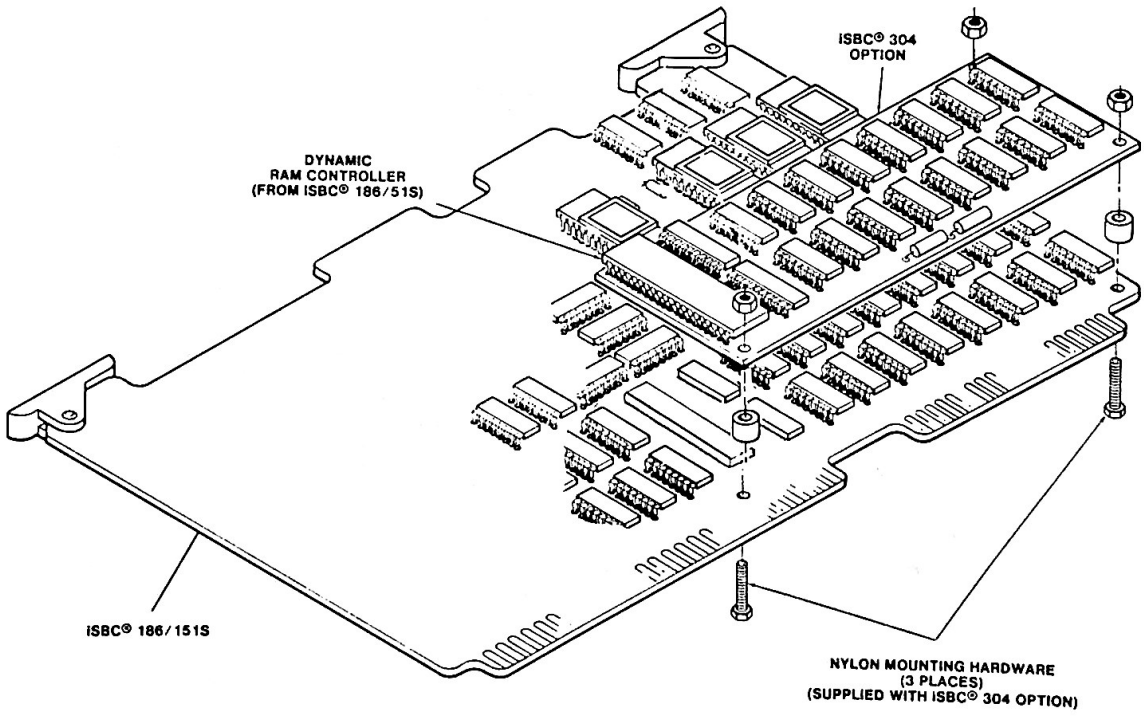
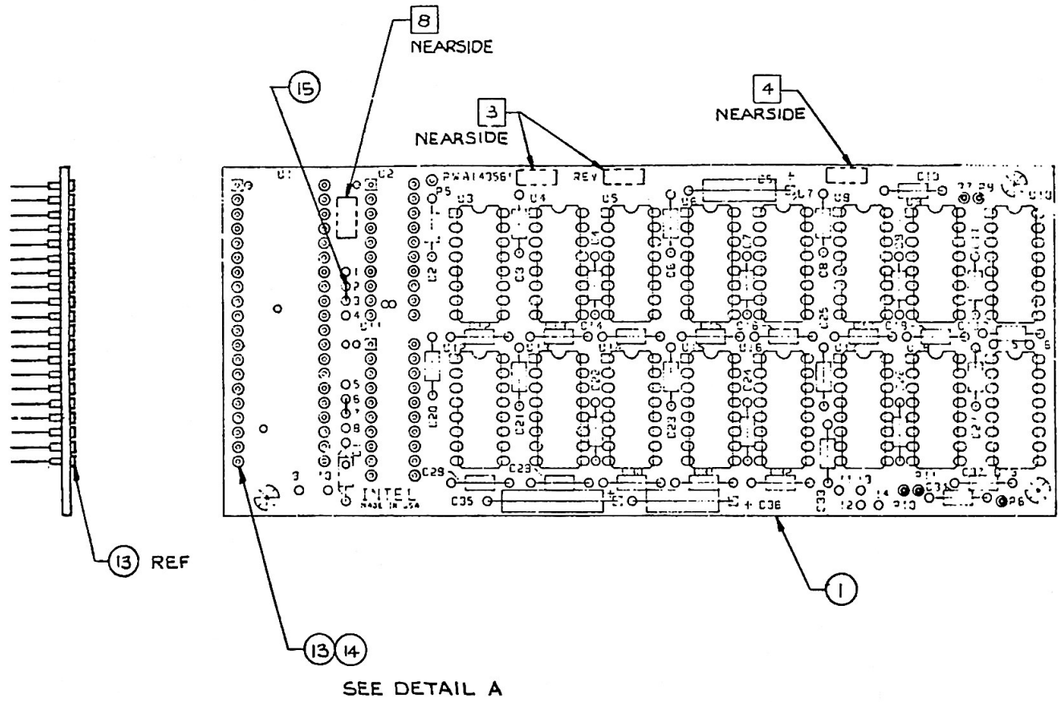
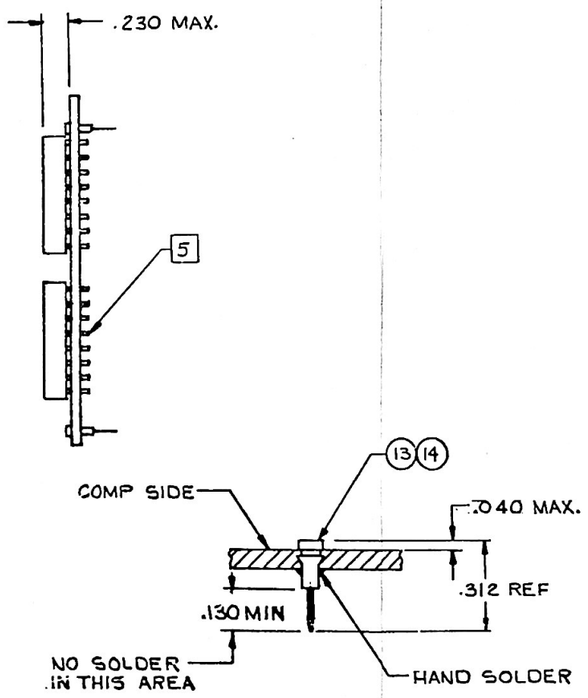


Figure A-1. iSBC® 304 RAM Expansion MULTIMODULE™ Board Orientation





DETAIL A

NOTES: UNLESS OTHERWISE SPECIFIED

1. PART NUMBER IS 143561-XXX.
2. THIS DOCUMENT, PARTS LIST AND WIRE LIST ARE TRACKING DOCUMENTS.
3. MARK ASSEMBLY DASH NUMBER AND REVISION LEVEL IN CONTRASTING PERMANENT COLOR, NON-CONDUCTIVE, .12 HIGH, APPROXIMATELY WHERE SHOWN.
4. MARK VENDOR ID WITH CONTRASTING PERMANENT COLOR, NON-CONDUCTIVE, .12 HIGH, APPROXIMATELY WHERE SHOWN.
5. TRIM I.C. LEADS AFTER ASSY TO .050 MAX.
6. U7, U2 AND U11 ARE SUPPLIED BY CUSTOMER.
7. WORKMANSHIP PER 99-0007-001.
8. MARK APPROPRIATE PRODUCT CODE (300, 300A, OR 304) WITH CONTRASTING PERMANENT COLOR, NON-CONDUCTIVE, .12 HIGH, APPROXIMATELY WHERE SHOWN.

Figure A-2. iSBC® 304 RAM Expansion MULTIMODULE™ Assembly Drawing

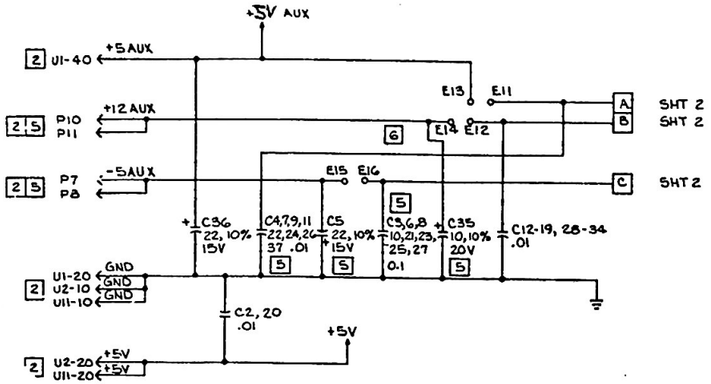


TABLE 1

PRODUCT		300		300A		304	
BOARD CAPACITY		32K		32K		128K	
MEMORY DEVICE		2117-4		2118-4		2164-20	
PIN NUMBER U3-10, U11-19	1	-5V AUX		N.C.		N.C.	
	8	+12V AUX		+5V AUX		+5V AUX	
	9	+5V AUX		N.C.		A7	
	16	GND		GND		GND	
JUMPERS		FROM	TO	FROM	TO	FROM	TO
		E15	E16	E12	E13	E12	E13
		E12	E14			E9	E10
		E11	E13				
MEMORY CONTROLLER		8202A		8202A		8203	
MEMORY CONTROLLER PIN	23	$\overline{RAS2}$		$\overline{RAS2}$		$\overline{OUT7}$	
	24	BØ		BØ		AL7	
	25	BI/OPI		BI/OPI		AH7	
	26	RAS3		RAS3		BØ	
	35	TNK		TNK		16K/$\overline{64K}$	

TABLE 2

$\overline{RAS}$ JUMPER TABLE				
$\overline{RAS}$ TO RAM	MEMORY DEVICE U3-U10		MEMORY DEVICE U12-U19	
	FROM	TO	FROM	TO
$\overline{RAS1}$	E2	E3	E6	E7
$\overline{RAS2}$	E1	E2	E5	E6
$\overline{RAS3}$	E2	E4	E6	E8

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C37	P1-4, 9
U19	
E16	
P11	

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL CAPACITOR VALUES ARE IN MICROFARADS, +80%, -20%, 50V.
2. THESE PIN CONNECTIONS MATE WITH SOCKETS ON iSBC HOST BOARD.
3. U1, U2 AND U11 ARE NOT SUPPLIED.
4. FOR $\overline{RAS}$ -TO-RAM JUMPERS SEE TABLE 2.
5. THESE COMPONENTS NOT INSTALLED ON 300A, OR 304.
6. FOR VOLTAGE JUMPERS SEE TABLE 1.
7. FOR PIN OUTS SEE TABLE 1.

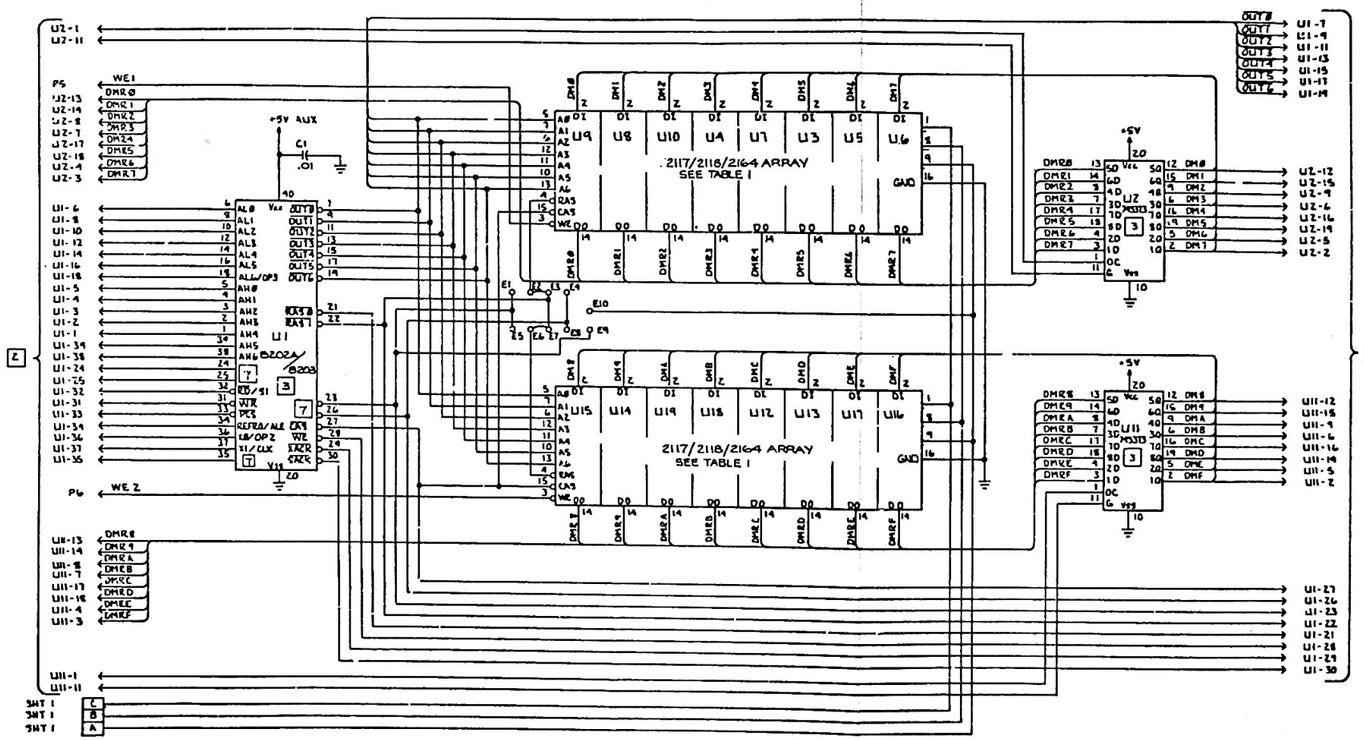


Figure A-3. iSBC® 304 RAM Expansion MULTIMODULE™ Schematic Diagram

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